Organic Electronics 15 (2014) 646–653

Contents lists available at ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel

Fabrication of a planar water gated organic field effect transistor using a hydrophilic polythiophene for improved digital inverter performance

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ARTICLE INFO

Article history:
Received 25 July 2013
Received in revised form 16 December 2013
Accepted 22 December 2013
Available online 4 January 2014

Keywords:
Water gated organic field effect transistor
Planar gate electrode
Polythiophene (P3HT) functionalized with poly(ethylene glycol)(PEG)
Hydrophilic semiconductor polymer
Transconductance of OFET
Gain of digital inverter

ABSTRACT

A planar water gated OFET (WG-OFET) structure is fabricated by patterning gate, source and drain electrodes on the same plane at the same time. Transistor output characteristics of this novel structure employing commercial regioregular poly(3-hexylthiophene) (rr-P3HT) as polymer semiconductor and deionized (DI) water as gate dielectric show successful field effect transistor operation with an on–off current ratio of 43 A/A and transconductance of 2.5 μA/V. These output characteristics are improved using P3HT functionalized with poly(ethylene glycol) (PEG) (P3HT-co-P3PEGT), which is more hydrophilic, leading to on–off ratio of 130 A/A and transconductance of 3.9 μA/V. Utilization of 100 mM NaCl solution instead of DI water significantly increases the on–off ratio to 141 A/A and transconductance to 7.17 μA/V for commercial P3HT and to 217 A/A and to 11.9 μA/V for P3HT-co-P3PEGT. Finally, transistors with improved transconductances are used to build digital inverters with improved characteristics. Gain of the inverters employing P3HT and P3HT-co-P3PEGT are measured as 2.9 V/V and 10.3 V/V, respectively, with 100 mM NaCl solution.

1. Introduction

Studies on organic electronics have continued to grow increasingly since the discovery of conductive polymers [1]. Organic electronics have benefits of low cost and simple fabrication methods and allows large-area production and usage of flexible substrates [2,3]. Also, many different semiconductor polymers can be synthesized and tailored for many different applications. Polymers can be functionalized as well to impart certain desired characteristics [4,5].

Many basic semiconductor devices, such as diodes [6], light emitting diodes [7], solar cells [8] and field effect transistors [9] are extensively explored in organic electronics. Among these, organic field-effect transistors (OFETs) are promising candidates for printed electronics in many applications such as displays, electronic paper, digital logic and radio frequency identification (RFID) tags [10]. Initial OFETs were typically built on silicon substrates that were insulated with thermally grown silicon oxide for testing, where silicon was the gate electrode and thermal oxide was the gate insulator [11]. Thin film insulating polymers [12] or self assembled monolayers [13] have also been used as gate insulators on different types of substrates. Inkjet printing methods have become common in the fabrication of OFETs [14]. P and n-channel operations have been demonstrated in OFETs, thus suggesting the possibility to built complementary circuits [15]. Thus, developed OFETs have been integrated to form simple and cheap circuits for RFID [16] and other electronic applications [6].

One of the major challenges of OFETs in integrated circuits is their low transconductances and high operating voltages. Since it is hard to form very thin, pin-hole free

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http://dx.doi.org/10.1016/j.orgel.2013.12.024

insulators in OFETs, source–drain voltages of around −40 V is typical in OFETs employing thermally grown SiO_2 with a thickness about 200 nm as gate insulator [11]. Inkjet-printed polymer transistors also operate at high voltages of around −20 and −40 V. In order to operate at voltage levels of 3 V, 2 V or below OFET must employ nanometer-thick gate insulator layers with a high dielectric constant [13]. However, ultra thin layers are impractical to use in printed electronics where robustness and cost is a major challenge. Thus, the development of printed electronics is facing a great challenge due to the lack of cost effective transistors and logic circuits that can operate at low voltages and have high voltage gains.

Since organic semiconductors have moderate carrier mobility values, in order to get satisfactory conductivities with low operating voltages such as 1 V or less, gate capacitance per area should be very high. A smart approach to solve this problem is to use electrolytes as gate insulator material [17]. In electrolyte-based OFETs, the capacitance which is created by migrated ions at the polymer surface is virtually independent of the thickness of the bulk of the electrolyte layer. This property makes electrolytes very attractive for use in organic electronic circuit applications [18,19]. This high capacitance is realized by the formation of an electrical double layer (EDL) and, is commonly referred to as electrical double layer capacitance (EDLC). Using an ion-conducting electrolyte as an OFET gate dielectric, it has been shown that the formation of EDLs at interfaces can be exploited to induce a very high charge carrier density in the channel of an OFET at low applied voltages [17]. Therefore, using electrolytes including ionic liquids, ion gels and even water as gate insulator meets the requirement of providing a simple and cheap way for the operation of OFETs below 1 V [20–22].

A simple water gated OFET (WG-OFET) example utilizes a manually immersed vertical probe as gate electrode as shown in Fig. 1a [22]. In this structure, semiconductor polymer coats the drain and source electrodes. A DI water droplet is placed on this hydrophobic polymer avoiding any contact with the electrodes. A gold, platinum or tungsten probe is then immersed into the droplet and used as gate electrode for field effect modulation. Due to electrical double layer capacitance formed at the electrolyte-semiconductor interface with typical values of tens of $\mu F/cm^2$, it is demonstrated that this transistor structure can function successfully below 1 V [17,22].

A problem that surfaces in the design mentioned above is that manual placement of the probe renders its location arbitrary. This often times causes problems in getting similar and repeatable results from devices manufactured in the same or a different batch. This limits their usage towards building basic logic circuits, such as inverters, or as chemical or biological sensors. Another problem is that WG-OFET in this structure cannot be easily integrated to each other or integrated to microfluidic channels. A top-gate electrode can be integrated to the ceiling of a microfluidic channel to constitute a compact electrode structure and confine the DI water to the microfluidic channel by capillary forces [23]. Such an encapsulation defines same active region area for each device [24]. However, fabricating such a device and then integrating many of them together to form an integrated circuit is very hard and complicated.

In this work, we disclose a novel WG-OFET configuration, where the gate electrode is planar with drain and source electrodes (Fig. 1b). In a previous work, Cho et al. has shown that vertical non-aligned gate electrode, which is formed after source and drain electrodes are patterned and ion gel is added, can still form a channel due to the high polarizability of ion gel dielectrics [25]. Here, we demonstrate the concept that gate electrode can be located on the same plane with source and drain electrodes. Hence, all of the electrodes can be patterned in a single step using a single mask. The polymer semiconductor coats the source-drain electrodes only, and does not make any contact with the gate electrode. The DI water droplet covers both polymer and gate electrode without making contact with source and drain electrodes. Since electrical double layer is formed over the active region, the carriers accumulate at this region and a channel is formed. The main advantage of this structure is that location of the gate electrode is highly controlled and it can be easily integrated to microfluidic channels.

Another problem of WG-OFET structure is that commonly used semiconductor polymers such as regioregular poly(3-hexylthiophene) (rr-P3HT) are hydrophobic. In WG-OFET device, semiconductor–water interface is the most crucial region. There can be discontinuities in this interface because of the hydrophobic nature of the polymer, which can lower the double layer capacitance, thus lowering the performance of the device [22]. This is evident from published results in literature. A structure of

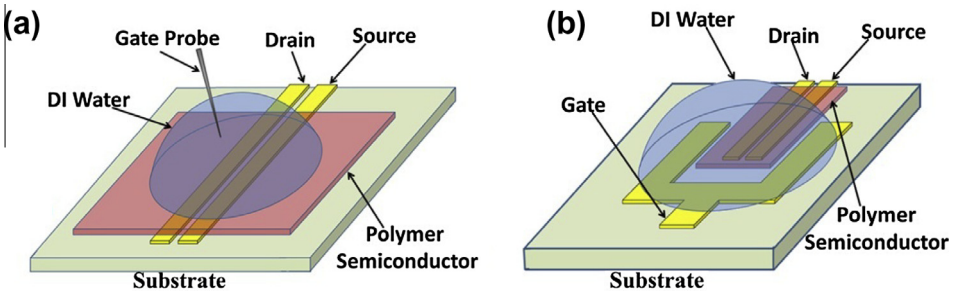

Fig. 1. Transistor architectures with probe gate (a) and planar gate (b).