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Defect-controlled synthesis of graphene based nano-size electronic devices using in situ thermal treatment

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ABSTRACT

Defect-controllable reduction approach of graphene is demonstrated. By in situ thermal reduction from graphene oxide on silicon wafer (300 nm SiO_2), large size (~15 μm) of single and few-layer graphene with highly improved electrical properties has been prepared. The effects of increasing annealing temperature on reducing the defect, restoring the lattice and enhancing the field-effect performance of graphene are proved. The characteristics of the sample were analyzed using optical microscope (OM), atomic force microscope (AFM), X-ray photoelectron spectra (XPS), Raman laser, semiconductor parameter analyzer and a micromanipulator. The devices based on the obtained few-layer graphene exhibit relatively high *p*-type transistor characteristics (6.2 $cm^2/V\,s$) in the atmospheric environment.

1. Introduction

Graphene is attracting intensive attentions owing to its fascinating physical properties such as quantum electronic transport [1,2], a tunable band gap [3], extremely high mobility [4], excellent ferromagnetic [5] and electromechanical modulation [6]. Nowadays, graphene is applied in many frontiers such as electrodes of supercapacitor [7–9], solar cell electrodes [10], lithium ion battery anodes [11], and optoelectronic applications [12,13]. Since the discovery of the first isolated graphene prepared by mechanical exfoliation of graphite crystals [14], many chemical approaches for synthesizing large-scale graphene have been developed, including chemical vapor deposition (CVD) [15], epitaxial growth on silicon carbide [16–18], chemical and thermal reduction of graphite oxide (GO) [19–22], and bottom-up organic synthesis [23]. Although CVD method has been widely applied in the preparation of graphene now, the product with the metal substrate cannot be used in microelectronics directly. Among these methods, the exfoliation of GO followed by reducing was proven to be an effective method to make graphene layers under the consideration of low cost, massive scalability [21], high-efficient production and aqueous stability. Chemical reduction appeared to be a suitable reduction approach. However, the application of reduced graphene oxide (rGO) in nano-size electronic device, such as field-effect transistors (FETs), is very limited. The inevitable defects of rGO should be the major barrier of its application in electronic devices. Meanwhile, the introduction of reductant impurities also affects the device performance. Recently, Dai et al. [24] investigated the contribution of temperature on the defect elimination of graphene during the chemical solution reduction, which suggested the higher temperature could be more favorable to obtain highly conjugated rGO. Similar result was also reported by Loh et al. [25].

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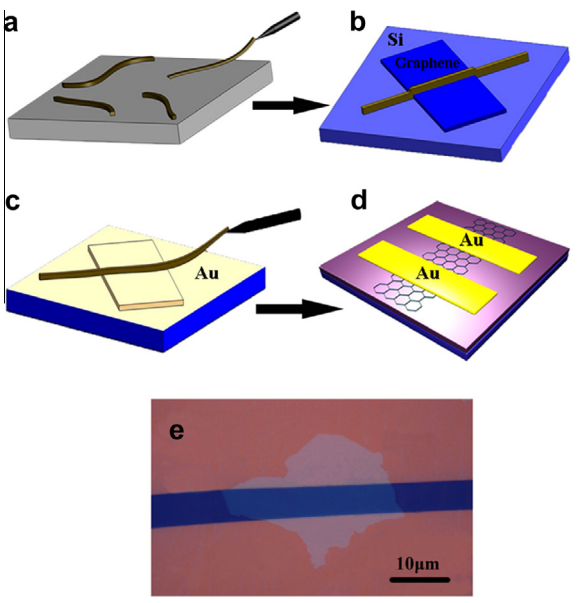
It is well-known that the different reduction processes of GO would result in different properties that in turn affect the final performance of device composed of graphene. Considering that thermal reduction by rapid annealing can effectively decompose oxygen-containing groups without introducing impurities and the reduction efficiency in an inert atmosphere would be higher than that in air, rapid thermal treatment of GO in Argon was carried out. The results indicate that the treatment temperature plays a very important role in the control in topological defects of rGO. By using the obtained rGO on SiO_2 substrate, FET nanodevice based on graphene has been easily prepared by "organic ribbon mask" technology as shown in Scheme 1 [26]. The field-effect experiment shows that the mobility is 6.2 cm^2/V s when the reduction temperature reaches 1000 °C, which has been improved remarkably compared with chemical solution reduced GOs (0.713 cm^2/V s). It is noteworthy that the reduction temperature should be no higher than 1000 °C owing to the electronics limitation.

2. Experimental section

2.1. Preparation of GO/silicon

Modified Hummer's method [27,28] was used to obtain graphite oxide from natural graphite. In a typical reaction, 5 g of graphite, 5 g of $NaNO_3$, and 150 ml of H_2SO_4 were added into a three-neck flask in an ice-water bath and mixed together with mechanical stirring. 15 g of $KMnO_4$ was then slowly added into the flask. The resulting suspension was moved to a water bath at 35 °C and stirred for about 6 h, forming a thick paste. Then 200 ml water was added and the suspension was stirred for 15 min while the temperature was raised to 95 °C. Finally, 700 ml of water was added, followed by the slow addition of more than 20 ml of H_2O_2 (30%) to remove excess $KMnO_4$, turning the color of the suspension from dark brown to yellow. The warm suspension was filtered and washed with a large amount of water. The filter cake was dispersed in water with mechanical stirring and the resultant suspension was centrifuged at 1000 rpm for 3–5 times. The supernatant was also centrifuged at 8000 rpm for 15 min to remove water-soluble byproducts and small graphite oxide pieces. The stable GO suspension was obtained by ultrasonicating the resulting graphite oxide in water, using a JY99-II DN ultrasonicator (Ningbo Scientz Biotechnology, China) at ~800 W. Prior to deposition of GO sheets, the silicon substrates were ultrasonically cleaned with deionized water and alcohol. A droplet of a water suspension of GO (0.1 mg/ml) was dropped onto the silicon substrate, and the substrate was gently moved into an oven and dried at 80 °C for 1 h to remove most of water.



Scheme 1. (a–d) Fabrication process of a FET device based on rGO; (e) OM image of the FET device.

2.2. Reduction of GO

A typical process for thermally deoxidizing GO is as follows: (1) A quartz tube furnace was evacuated to 2 Pa and its temperature was maintained at 400 °C; (2) The GO/silicon sample was placed into the furnace with argon (500 sccm) flow for 5 min, maintaining the total pressure lower than 600 Pa; (3) the thermally deoxidized sample was taken from the hot-zone of the furnace using a rod with a hook and fast cooled to room temperature under argon atmosphere. The thermal deoxidizing process was carried out at 400, 600, 800 and 1000 °C in the same sample with in situ method. Here we should point out that the temperature is no more than 1000 °C owing to the requirement of device. The resultant samples were designated G-400, G-600, G-800 and G-1000, where the numbers indicate the annealing temperatures used. Graphene during chemical solution reduction (SrGO) was obtained with modified Dai's method [24] as a comparison. 50 μl of hydrazine monohydrate was added to 20 ml of the diluted GO/H_2O suspension (0.1 mg/ml) for reduction. The reduction was carried out in 50 ml autoclaves at 180 °C for 12 h. The suspension was still homogeneous after reduction. The rGO/H_2O suspension after reduction was spin-coated (2000 rpm, 20 s, 3 times) onto substrates (Si with 300 nm SiO_2 on top) for subsequent testing sample preparation.

2.3. The preparation of rGO/SiO_2/Si FET devices

The rGO based FET device was fabricated by using SiO_2/Si substrate as an back-gate electrode. The thickness of the dielectric layer is 300 nm. Au is selected as the source and drain electrode. Scheme 1 shows the fabrication process of FET. First, rGO was transferred onto the SiO_2/Si substrate. An organic strip was then peeled off from the glass substrate (Scheme 1a) by the mechanical probe and transferred onto the rGO flake to serve as the mask for the next Au deposition (Scheme 1b). Then, a 20 nm Au film was deposited on the substrate by using an ULVAC VPC-260F metal evaporation plating instrument as source and drain electrode (Scheme 1c). Finally, the organic mask strip was peeled off from the surface of the rGO flake and a