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Letter

Voltage-readable nonvolatile memory cell with programmable ferroelectric multistates in organic inverter configuration

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ABSTRACT

We demonstrate a voltage-readable nonvolatile memory cell with programmable ferroelectric multistates in an organic inverter configuration. The intermediate memory states of a ferroelectric gate insulator, varying with the magnitude of the programming voltage, allow the multilevels of the drain current at zero gate-source voltage in a ferroelectric organic field-effect transistor (OFET). The current output from the ferroelectric memory is directly converted into the voltage-readable output in a zero-gate load inverter configuration where both a driving paraelectric OFET having a paraelectric buffer layer and a load ferroelectric OFET are monolithically integrated in a single substrate. The multilevel voltage-readable output characteristics are obtained from the ferroelectric multistates as a function of the programming voltage.

Ferroelectric organic field-effect transistors (FeOFETs) have been paid much attention from the potential for the nonvolatile data storage at low cost and the design flexibility [1,2]. The underlying principle of the FeOFET memory comes mainly from the ferroelectric nature of a gate insulator wherein two dipolar alignment directions exist depending on the polarity of an applied electric field. As a result, two memory states corresponding to the two dipolar directions in the FeOFET enable to construct data storage devices with the binary nonvolatile memory [1–3]. Recently, for the massive data storage purpose, more than a single bit (two memory states) per memory cell is desirable and thus the FeOFET capable of storing multibit information provides one of the promising routes to the expansion of the memory capacity. The intermediate states between two completely aligned dipolar states in the FeOFET, for example, three memory states [4] and four memory states [5] have been recently reported.

In all of the existing FeOFETs [1–5], the stored information whether binary or multiple memory states is read in terms of the drain current owing to the inherent current output (I_{OUT}) nature of the FeOFET. As shown in Fig. 1a, the memory states associated with the dipolar alignment are dictated by the programming voltage (V_P) and read in terms of the drain current by the application of the source–drain voltage. However, for certain microelectronic applications requiring stable multistage operation [6,7], the voltage-readable output from the memory state is more preferred than the current output. Therefore, in addition to the multistate capability, the voltage-readability of the memory output is very important for a wide range of practical applications of the nonvolatile ferroelectric memory.

In this work, we demonstrate the voltage-readable nonvolatile memory cell with programmable ferroelectric multistates in an organic inverter-type configuration. In our inverter-type memory cell where both a driving paraelectric organic field-effect transistor (DPT) having a paraelectric buffer layer (PBL) and a load ferroelectric organic field-effect transistor (LFT) are laterally constructed in a single substrate, the current output from the FeOFET is converted into the voltage-readable output from the inverter as shown in Fig. 1b. The memory states preprogrammed by V_P are readable from the node in terms of the voltage output (V_{OUT}) which corresponds to a fraction

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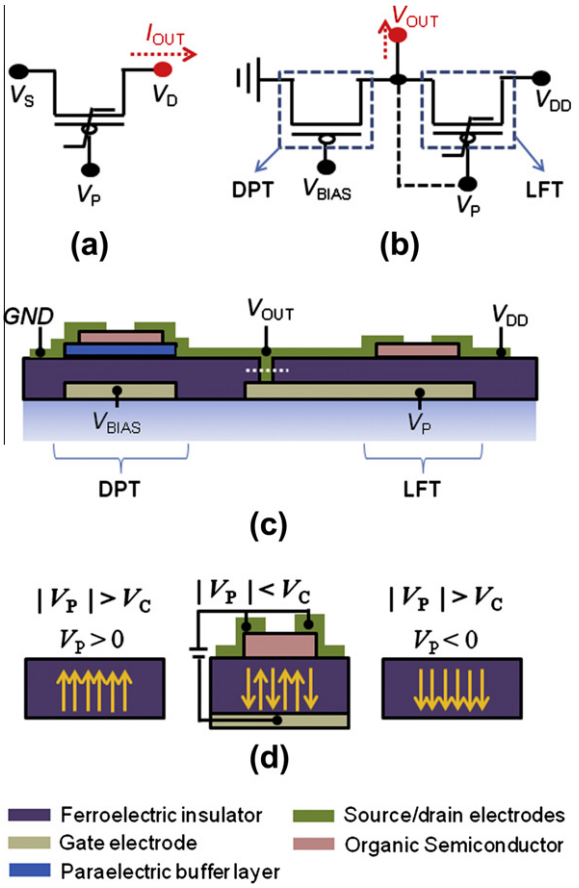

Fig. 1. (a) The circuit diagram of a FeOFET. The current at the drain electrode is read as the output current (I_{OUT}). The source voltage, the drain voltage, and the program voltage are denoted by V_S, V_D, and V_P, respectively. (b) The circuit diagram of an inverter-type ferroelectric memory cell consisting of a zero-gate load ferroelectric thin-film transistor (LFT) and a driving paraelectric thin-film transistor (DPT). The voltage at the node of interconnection (represented by a whitr dotted line) is read as the output voltage (V_{OUT}). The supply voltage and the bias voltage are represented by V_{DD} and V_{BIAS}, respectively. (c) The schematic diagram showing the cross-sectional view of an inverter-type ferroelectric memory cell consisting of the LFT and the DPT. The ground is denoted by GND. (d) The schematic illustration of typical dipole states in the ferroelectric insulator of the FeOFET: two fully aligned states of $V_P > 0$ (left) and $V_P < 0$ (right) under the condition that $|V_P| > |V_C|$ with the coercive voltage V_C. One of the intermediate (partially aligned) states between two fully aligned states: $|V_P| < |V_C|$ (middle). The arrows represent the dipole moments in the ferroelectric insulator.

of the supply voltage (V_{DD}). The magnitude of V_{OUT} depends on the relative channel resistance of the LFT to the DPT. In addition, the output current of the DPT is controlled by the bias voltage (V_{BIAS}) or the input voltage, meaning that the effective channel resistance depends on V_{BIAS}.

As shown in Fig. 1c, our approach is based on the introduction of the PBL for the monolithic integration of both the DPT and the LFT into a single substrate within the framework of the screening effect on the ferroelectric insulator. The node of the DPT and the LFT in a zero-gate load inverter configuration is represented by the white dotted in Fig. 1c. Moreover, for the LFT, the ferroelectric intermediate states between two fully aligned (up and down) states are realized by V_P in relative to the coercive voltage (V_C) [1,3] as shown in Fig. 1d. Under the condition that $|V_P| < V_C$, the reversal of the dipole moments in the ferroelectric insulator depends on the magnitude of V_P, resulting in different values of the net polarization. Accordingly, the multilevels of the drain current in the intermediate states of the LFT are converted into the multilevels of the output voltage from the inverter-type ferroelectric memory cell.

We constructed an inverter-type nonvolatile memory cell consisting of an LFT and a DPT as shown in Fig. 1c. Glass substrates were cleaned with acetone, iso-propylalcohol, methanol and deionized water in sequence. For a gate electrode, aluminum (Al) was thermally deposited on a cleaned glass substrate through a shadow mask. For preparing a ferroelectric gate insulator, poly(vinylidene fluoride) copolymer with trifluoroethylene (75/25 mol%) copolymer [P(VDF-TrFE)], dissolved in cyclopentanone in 10 wt%, was spin-coated on the substrate and subsequently cured at 140 °C (just above the Curie point) for 2 h to promote the ferroelectric β-phase of the P(VDF-TrFE) film [8]. The thickness of the P(VDF-TrFE) film was measured as 630 nm. In fabricating the DPT, a fluorinated polymer (NovecTM EGC-1700, 3M), which is paraelectric and compatible with transfer-printing, was chosen as the PBL. The PBL pattern was transfer-printed onto the ferroelectric gate insulator using an elastomeric stamp without heat and/or high pressure [9,10]. The thickness of the PBL was 50 nm. For the interconnection of the DPT with the LFT in the inverter-type configuration, a via-hole was produced using a solvent-drop method [9]. An organic semiconductor of pentacene was simultaneously deposited on the PBL for the DPT and the ferroelectric gate insulator for the LFT by thermal evaporation at the rate of 0.5 Å s^{-1} under the pressure of about 10^{-6} Torr. The thickness of the pentacene layer was about 50 nm. For the source/drain electrodes, thermal deposition of gold (Au) was carried out at the rate of 1.0 Å s^{-1} under the pressure of about 10^{-6} Torr, producing the Au layer of 65 nm thick. The length and the width of the active channel were 50 μm and 1000 μm, respectively. The DPT and the LFT were interconnected through a via-hole to produce a zero-gate load inverter after the LFT was preprogrammed by V_P. In this case, the read-only-memory is available. Note that the rewritable memory can be also realized provided that the memory states of the LFT are reprogrammable. The reprogramming process can be performed in the gate-source disconnected state. The measurements of the electrical properties of the LFT, the DPT, and the resultant inverter were carried out using a semiconductor parameter analyzer (HP4155A, Hewlett–Packard Co.) under ambient pressure at room temperature and an elevated temperature of 70 °C.

Let us first examine the electrical properties of the FeOFET with the PBL on the ferroelectric P(VDF–TrFE) insulator. In contrast to strong hysteresis in conventional FeOFETs [2,3,8], the transfer curve of the FeOFET with the PBL exhibits nearly negligible hysteresis as shown in Fig. 2a. This is attributed to the depolarization field generated the PBL [11]. In other words, the PBL plays an essential role in screening the dipolar interactions at the interface between the active layer and the gate insulator. Such