Organic Electronics 15 (2014) 1458–1464

Contents lists available at ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel

Role of ultrathin Al_2O_3 layer in organic/inorganic hybrid gate dielectrics for flexibility improvement of InGaZnO thin film transistors

Byeong-Ung Hwang [a], Do-Il Kim [a], Sung-Won Cho [a], Myeong-Gu Yun [a], Hak Jun Kim [b], Youn Jea Kim [b], Hyung-Koun Cho [a], Nae-Eung Lee [a,c,*]

[a] Department of Advanced Materials Science & Engineering, Sungkyunkwan University, Suwon, Gyeonggi-Do 440-746, Republic of Korea
[b] Department of Mechanical Engineering, Sungkyunkwan University, Suwon, Gyeonggi-Do 440-746, Republic of Korea
[c] SKKU Advanced Institute of Nanotechnology (SAINT), Sungkyunkwan University, Suwon, Gyeonggi-Do 440-746, Republic of Korea

ARTICLE INFO

Article history:
Received 4 November 2013
Received in revised form 17 March 2014
Accepted 4 April 2014
Available online 20 April 2014

Keywords:
Flexible device
a-IGZO
Hybrid gate dielectrics
Thin film transistors

ABSTRACT

We investigated flexible amorphous InGaZnO (*a*-IGZO) thin film transistors (TFTs) on a polyimide (PI) substrate by using organic/inorganic hybrid gate dielectrics of poly-4vinyl phenol (PVP) and ultrathin Al_2O_3. IGZO TFTs were fabricated with hybrid PVP/Al_2O_3 gate dielectrics having Al_2O_3 layers of different nanoscale thicknesses, which were deposited by atomic layer deposition (ALD). The electrical characteristics of the TFTs with the organic/inorganic hybrid gate dielectrics were measured after cyclic bending up to 1,00,000 cycles at the bending radius of 10 mm. The ultrathin Al_2O_3 layer in the hybrid gate dielectrics improved the mechanical flexibility and protected the organic gate dielectric against damage during the sputter deposition of the IGZO layer. Finite elements method (FEM) simulations along with the structural characterization of the cyclically bent device showed the importance of optimizing the thickness of the Al_2O_3 layer in the hybrid gate dielectrics to obtain mechanically stable and flexible *a*-IGZO TFTs.

1. Introduction

Recently, flexible electronics including thin film transistors has received considerable attention. In particular, TFT backplanes, including organic and metal oxide emiconductor channel TFTs as well as amorphous silicon (*a*-Si) and polycrystalline silicon (poly-Si) channel TFTs, have been extensively researched for flexible displays [1–3]. However, many active materials such as organic semiconductor and *a*-Si still have limitations due to their limited carrier mobility of the channel materials. Although poly-Si TFTs show superior electrical performance, it generally needs to be deposited or annealed at an elevated temperature [4]. Poly-Si based TFTs fabricated on a polymer substrate are still one of candidates for flexible backplanes due to their excellent electrical performance. In this case, however, structural engineering adopting the concept of mechanical neutral plane [5] or islanded morphology [6] needs to be applied because the materials in poly-Si TFTs are brittle.

As replacement for the poly-Si channel, transition metal oxide (TMO) materials have been considered because they have a high carrier mobility even in amorphous phase. Furthermore, oxide semiconductors can be deposited at lower temperatures, making them compatible with polymeric substrate. In addition, their special properties, such as optical transparency in the visible range due to a wide band gap, have also been investigated for transparent electronics. Especially, multi-component oxide semiconductors, realized by doping, have been investigated because of the

* Corresponding author at: Sungkyunkwan University, Suwon, Gyeonggi-Do 440-746, Republic of Korea.
E-mail address: nelee@skku.edu (N.-E. Lee).

http://dx.doi.org/10.1016/j.orgel.2014.04.003
1566-1199/

difficulty in controlling the carrier concentration in a two-component system such as ZnO due to oxygen vacancies. Among the multi-component system materials, amorphous indium–gallium–zinc oxide (*a*-IGZO) has been highly regarded for the active layer in flexible TFTs because of its high field-effect mobility, high current on/off ratio, and moderate resistance to mechanical stress [7–13].

For the realization of flexible electronics, the aforementioned mechanical neutral plane method, which places the active layer in the device at mechanical neutral plane, was demonstrated to reduce the mechanical stress on flexible devices [5]. A small islanded structure can also lead to the reduction of strain-induced failure of a device [6]. However, even when those methods are adopted in the fabrication of a flexible display, the characteristics of flexible TFTs can be degraded at an extremely small bending radius, because some layers would still be under mechanical stress. In particular, inorganic dielectric layers such as SiO_2, Si_3N_4, which are often deposited globally on a TFT backplane, are vulnerable to mechanical stress. And they can fail easily by cracking or delamination during repetitive large mechanical deformation.

In order to overcome the limits of the concept of mechanical neutral plane or islanded structuring, intrinsically flexible materials need to be obtained by synthesizing new materials [14], laminating organic and inorganic layers [15–17] or forming organic–inorganic nanocomposites [18]. These new materials can improve the flexibility as well as the electrical performance of TFTs. In the case of *a*-IGZO TFTs, sputter deposition is widely used. However, high energy sputtered particles easily induce damage on the pre-deposited layers, such as the organic gate dielectrics in bottom gated TFTs. Sputtering-induced damages even on flexible organic gate dielectrics gives rise to leakage current in TFTs. Hence, inorganic dielectric materials strongly bonded to organic dielectric materials have been proposed for bottom gated oxide TFTs [16,19,20]. However, even with high resistance against sputtering damage, inorganic materials too are easily cracked by repetitive mechanical deformation.

Therefore, the improvement of gate dielectric materials in flexible oxide TFTs by hybridization of organic and inorganic materials has become of great interest [16,19–21]. Even though a thick inorganic material may be brittle, an ultrathin inorganic layer can tolerate high mechanical stress. In this study, we investigated flexible *a*-IGZO TFTs with a hybrid gate dielectric of organic and inorganic film layers. The results indicated that the thickness of the inorganic gate dielectric layer is a critical factor in determining the mechanical stability and electrical performance of a device. The fabricated oxide TFT with a laminated multilayer gate dielectric having a ultrathin inorganic dielectric layer of 20 nm thickness showed high flexibility under repetitive mechanical deformation.

2. Experimental

A cross-sectional illustration of the *a*-IGZO TFT structure used for the cyclic bending experiment is shown in Fig. 1(a). Inverted-staggered top-contact IGZO TFTs were fabricated on a 125 μm-thick PI film (Du Pont; Kapton®) with a surface area of 2 cm × 7 cm. The substrates were cleaned in acetone, ethanol and de-ionized (DI) water by an ultra-sonicator. Then, the PI substrates were dried on a hot plate at 110 °C for 30 min to remove water vapor. Next, a PVP layer of 1 μm was spin coated on the PI substrates to make a smooth surface with root-mean-squared surface roughness of as low as 8 nm, which was required for the formation of high quality active layers. Then, a Ni gate electrode of 100 nm was deposited on the bare PVP layer by the *e*-beam evaporator system using a shadow mask. The PVP and Al_2O_3 layers of different thicknesses were formed by spin coating and ALD at 200 °C, respectively. Especially, the Al_2O_3 layer plays an important role in protecting the organic gate dielectric layer against sputtering damage during sputter deposition of the oxide semiconductor layer. A 50-nm-thick active layer (*a*-IGZO target; In_2O_3: Ga_2O_3: ZnO = 1:1:1 mol%) was deposited by RF sputtering at power of 100 W and working pressure of 5 mTorr in 1% O_2/(Ar + O_2) atmosphere at room temperature. Following the deposition of the oxide semiconductor layer, Al source/drain electrodes of 70 nm thickness were deposited by thermal evaporation using a shadow mask. Then, the fabricated devices were annealed on a hot plate at 200 °C for 1 h. To minimize the ambient effects from the air atmosphere during the cyclic bending test, the fabricated devices were encapsulated with a 100-nm-thick tetratetracontane (TTC) layer, deposited by thermal evaporation at 50 °C.

TFTs were tested by loading them between two parallel plates in the cyclic bending tester. Flexibility test using cyclic bending was performed in the tension mode at a bending radius of 10 mm. The electrical characteristics of the TFTs before and after the bending test were evaluated in air atmosphere using an HP 4145B (Agilent Technologies) semiconductor parameter analyzer. Then, the TFTs were examined by optical microscopy and a dual-type focused ion beam (FIB) scanning electron microscope (SEM) to confirm any cracking or delamination of the device layers.

Stress and strain distributions in the TFT device structures were systematically analyzed using the finite elements method (FEM). A problem-specific numerical model used to simulate the strain and stress on the device was validated numerically using a commercially available computational package, COMSOL (Altsoft, Inc.). Fig. 1(b) shows the bending simulation of the *a*-IGZO TFT with a hybrid gate dielectric. To analyze deformation and structural loads in the *x*- and *y*-directions, the *a*-IGZO TFT was developed into a two-dimensional (2D) structure, wherein the *z*-component of the strain was assumed to be zero. For subsequent analysis of the strain–stress interaction, a 2D plane stress application mode was used. The lower corners of both sides of the PI substrate were fixed in the *x*- and *y*-directions, respectively. The structural characteristics of the *a*-IGZO TFT were estimated for a forced load of 100 N in the *x*-direction. The upper layers, excluding the PI substrate layer, were analyzed as a narrow region in the *y*-direction. The mapped mesh method was applied to generate numerical meshes of quadrilateral elements over all the layers. The grid systems and the degrees of freedom for all the layers were 360–370 elements, respectively.