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Numerical analysis of capacitance compact models for organic thin-film transistors

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ABSTRACT

Analytical expressions for the gate-voltage dependence of the channel capacitance and the gate-to-contacts overlap capacitances in top-contact organic thin-film transistors (OTFTs) are derived and implemented in an organic compact capacitance model. The resulting modified model is verified by experimental data of transistors with constant mobility. The same model is analyzed by numerical simulations for OTFTs with a voltage-dependent mobility. The simulation results indicate that the quasistatic model describes well the simulated capacitances. In accumulation, the modeled values are slightly overestimated because of the generally accepted assumption of the charge-sheet model. It is also demonstrated that the quasistatic regime occurs at lower frequencies because of the reduced mobility at lower charge carrier concentrations.

1. Introduction

In recent years substantial efforts have been made in the fabrication and performance of discrete OTFTs. For commercial applications of these transistors in organic integrated circuits reliable compact models that allow the description of the electrical transistor behavior are required. The static properties are described by current–voltage (I–V) characteristics. Therefore, several DC models were developed and verified by experimental data [1–7]. In these models the increase of the mobility with the gate-source voltage was considered. Whereas in [2,4,7] this mobility model was explained by the charge trapping in deep tails of distributed states described by Shur and Hack [8], in [1,3,5,6] the model of the variable range hopping (VRH) in an exponential distributed density of states (DOS) [9] was assumed.

The dynamic behavior is determined by the intrinsic and parasitic capacitances so that capacitance models are necessary for the description. Contrary to the DC models, the developed capacitance compact models of organic transistors were not verified by experimental data since measurements of OTFTs in the quasistatic regime were not available [1,3,5,10,11]. The common point of these models is again the consideration of the special mobility dependence on the gate-source voltage. As a consequence, similar expressions have been derived with minor diverging model parameters. This is confirmed in [11] where the therein derived expressions are compared to the results given in [1]. Differences of the models are related to the consideration of the overlap regions. For instance, no expressions for the overlap capacitance are given in [1,3,5]. In contrast, in [11,10] this capacitance is discussed

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more in detail but gate- and drain-voltage-independent equations are finally assumed. Such expressions are only valid in a source/drain (S/D) bottom-contact configuration. However, OTFTs are often prepared in a bottom-gate and S/D top-contact (TOC) design as it offers a reduced contact resistance [12,13]. In this configuration the S/D contacts are on top of the organic layer with the result that the overlap capacitances are voltage-dependent.

In [17] the measured gate-source (C_{gs}) and gate-drain (C_{gd}) capacitances of the prepared OTFT with constant mobility were modeled assuming the simple Meyer's capacitance model [18] and constant overlap capacitances despite of the TOC design.

In this paper, we derive an expression to consider the gate- and drain-voltage dependence of the gate-to-contacts overlap capacitances in S/D TOC transistors. This equation and a gate-voltage dependent channel capacitance (an expression similar to the one in [18]) are implemented in the organic capacitance model of [11] originated from the DC model in [6] in which the mobility enhancement factor is explained either by charge trapping or by VRH in an exponential DOS. The influence of contact resistance effects, such as described in [14–16], are not considered in this paper.

For organic transistors with a constant mobility, the modified model is verified against experimental data adopted from [17]. For transistors with a voltage-dependent mobility, the model of Marinov and Deen [11] is verified by two-dimensional device simulations in the quasistatic regime. For this purpose, the voltage-dependent mobility model for VRH in an exponentially distributed DOS [19] was implemented in the Sentaurus Device simulator [20]. Furthermore, the frequency dependence of the transistor capacitances was investigated by the simulation. From these results, the frequency was estimated up to which the quasistatic assumption is valid for the OTFT.

2. Transistor fabrication

OTFTs in a bottom-gate/top-contact design are prepared on an alkali-free glass substrate covered with a thin (4 nm) adhesion layer of aluminum oxide [17]. The hybrid dielectric on top of the aluminum gate consist of an oxygen-plasma-grown AlO_x layer (3.6 nm-thick) and a solution-processed self-assembled monolayer (SAM) of n-tetradecylphosphonic acid (1.7 nm-thick). The active layer of the OTFT, namely the 11-nm-thick organic semiconductor (OSC) dinaphto[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) [21] and finally 25-nm-thick gold S/D contacts were evaporated through silicon stencil masks [22]. The transistors have a channel length and width of $L = 200\ \mu m$ and $W = 400\ \mu m$, respectively. The gate-to-source (L_{gs}) and gate-to-drain (L_{gd}) overlaps are symmetrical with $L_{gs} = L_{gd} = 10\ \mu m$.

3. Simulation method

Numerical simulations have been carried out with the Sentaurus Device simulator solving the Poisson and continuity equations [20]. To investigate the OTFT capacitances a small-signal analysis was performed. In this case, the response of the device to small sinusoidal signals superimposed upon an established DC bias is computed as a function of frequency and DC operating point. The result is a complex admittance matrix. The simplified simulated structure is shown in the inset of Fig. 1. The used parameters are summarized in Table 1. The values for the relative permittivity of the insulator, the DNTT thickness and the doping concentration were extracted from the measured capacitance–voltage curve for a drain-source voltage $V_{DS} = 0$ V (shown in [17]). The concentration of fixed interface states was assumed to fit the flat-band voltage (V_{FB}). With the given parameters and $V_{TH} = V_{FB} + eN_A d/C''_{is}$ a threshold voltage of $V_{TH} = -1.2$ V results. C''_{is} is the insulator capacitance per area. The intrinsic mobility was estimated from measured current–voltage characteristics of the OTFT [17]. For these transistors no dependence of the mobility on the gate-source voltage was observed.

For the investigation of the capacitance model derived in [11], the voltage-dependent mobility model described in [19] was implemented. This model is based on the hopping model of [9] only modified by the lateral field dependence.

4. Experimental and simulated results

As described above, in [17] the measured capacitances of the OTFTs were modeled with the Meyer's capacitance model [18]. Here, the quasistatic capacitance model

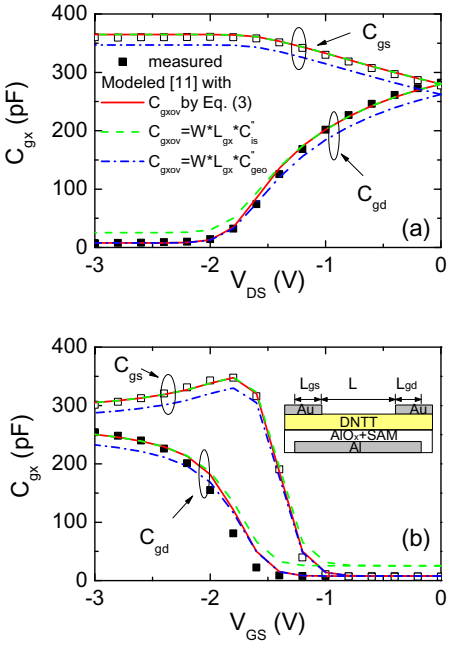

Fig. 1. Data adopted from [17] at a frequency of $f = 500$ Hz and modeled quasi-static gate-source (C_{gs}) and gate-drain (C_{gd}) capacitances as a function of V_{DS} with $V_{GS} = -3$ V (a) and V_{GS} with $V_{DS} = -0.5$ V (b), respectively. Lines represent the model by [11] including the voltage dependence of the channel capacitance, a constant fringe part of 13% and the indicated equations of the overlap capacitances. The inset shows the OTFT schematic representation used for the simulation.