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Intrinsic difference in Schottky barrier effect for device configuration of organic thin-film transistors

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ABSTRACT

Schottky barrier effect for n-channel organic thin-film transistors (OTFTs) with bottom-gate, top-contact (TC) and bottom-gate, bottom-contact (BC) configuration was examined by using device simulation with a thin-film organic transistor advanced simulator (TOTAS). A thermionic field emission (TFE) model which addresses tunneling of thermally excited electrons was applied as a carrier injection model of OTFTs. Simulation results reveal that the BC configuration is affected by Schottky barrier more severely than the TC configuration under the same condition for device parameters, and that this discrepancy in device characteristics can be completely alleviated by contact-area-limited doping, where highly-doped semiconducting layers are prepared in the neighborhood of contact electrodes. Moreover, the existence of an intrinsic Schottky barrier is indicated even though an ohmic-contact condition is assumed, which becomes more prominent for lower bulk carrier concentration in organic semiconductor. This work suggests the availability of the TFE model for simulating realistic OTFT devices with Schottky contacts. From the simulation results, intrinsic differences in device performance for the TC and BC configurations are discussed.

1. Introduction

Metal/organic heterointerfaces have been widely studied in terms of both scientific and practical viewpoints. In the area of surface science, some charge transfer interactions between metals and molecules [1], and thereby new electronic states and phenomena such as vacuum level shift [2] are discussed in detail. In practical aspects, in organic electroluminescence (EL) devices [3–5] and thin-film transistors (OTFTs) [6–8], carrier injection from contact electrodes to organic semiconductor layers is usually governed by Schottky energy barriers formed at metal/organic heterointerfaces [9,10]. Therefore, in device design based on realistic organic thin-film devices, Schottky contacts should be introduced into conventional device simulations by employing an appropriate physical model. In previous studies, we employed a thermionic field emission (TFE) model as a carrier injection mechanism for two-dimensional device simulation of OTFTs [11]. The TFE model expresses tunneling of thermally excited electrons at a reverse-biased Schottky contact [12,13], and is thought to be well suited for incorporating carrier tunneling injection into device simulation. Actually, electrical characteristics in realistic OTFTs with Schottky barriers can be reproduced well with our simulation technique [11].

In this work, we performed device simulation for n-channel OTFTs with different device configurations by incorporating the TFE model into device simulation. Two device configurations were examined; bottom-gate, top-contact (TC) and bottom-gate, bottom-contact (BC) configuration. The TC configuration is the most widely

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used for evaluating the carrier mobility of semiconductor materials, while the BC configuration is suitable for forthcoming flexible-device application because of its easy fabrication on any plastic substrate with higher device densities. Simulation results suggest an intrinsic discrepancy in contact resistance between top- and bottom-contact OTFTs, and this discrepancy can be mitigated by carrier doping around the contact areas (called contact-area-limited doping [14–21]). From the results in this study, the difference in Schottky barrier effect for device configuration of OTFTs is discussed.

2. Device simulation

2.1. OTFT simulation with Schottky contact

Current–voltage characteristics, and cross-sectional distributions of potential and carrier concentration in n-channel OTFTs were calculated with a thin-film organic transistor advanced simulator (TOTAS) [22–24], where a finite difference method is employed and a set of discretized Poisson's and current continuity equation is solved by a full Newton method. For OTFT simulation with Schottky contacts, the following current density equations derived from the TFE mechanism at electrode/semiconductor heterointerface were utilized as boundary conditions for the current continuity equation:

$$J = J_S\left(\exp\left(\frac{-E}{\varepsilon'}\right) - 1\right) \quad (-E = qV_R), \tag{1}$$

$$J_S = \frac{A\sqrt{\pi E_{00}}}{kT}\sqrt{-E + \frac{q\phi_B}{\cosh^2(E_{00}/kT)}}\exp\left(-\frac{q\phi_B}{E_0}\right), \tag{2}$$

where V_R is the reverse bias applied to the semiconductor bulk ($V_R > 0$), q is the elementary charge, k is the Boltzmann constant, and T is the absolute temperature (300 K). A is the classical Richardson constant given by $A = 4\pi m^* q(kT)^2/h^3$, where m^* is the effective electron mass and h is the Planck constant. ϕ_B is the barrier height defined as the difference between the work function of the contact metal and the energy of the electron transport level in the semiconductor. The current density in Eq. (1) is given in a slightly different form from that in the original literature [12] ($J = J_s \exp(-E/\varepsilon')$) in order to obtain solutions for a neighborhood of zero bias. The energy parameters of ε', E_0, and E_{00} appearing in Eqs. (1) and (2) are written as

$$\varepsilon' = \frac{E_{00}}{\frac{E_{00}}{kT} - \tanh\left(\frac{E_{00}}{kT}\right)}, \tag{3}$$

$$E_{00} = \frac{2q}{\alpha}\sqrt{\frac{N_D}{2\varepsilon_S\varepsilon_0}}, \tag{4}$$

$$\alpha = \frac{4\pi\sqrt{2m^*}}{h}, \tag{5}$$

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{kT}\right). \tag{6}$$

Here, N_D is the impurity concentration of the semiconductor, ε_S is the dielectric constant of the semiconductor, and ε_0 is the dielectric permittivity of vacuum.

In addition, for Poisson's equation, the following fixed boundary condition for the potential is introduced:

$$\psi = V_0 + \frac{kT}{q}\ln\left(\frac{N_C}{n_i}\right) - \phi_B, \tag{7}$$

where ψ is the potential at Schottky contact, V_0 is the applied bias to the source electrode ($V_0 = 0$), N_C is the effective

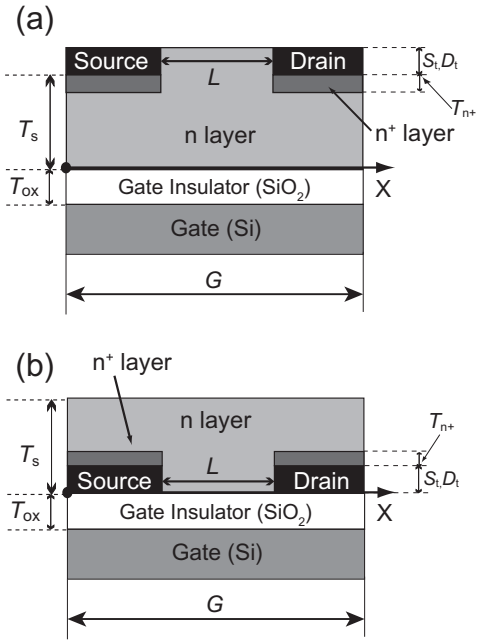

Fig. 1. Schematic cross section of (a) bottom-gate, top-contact (TC) and (b) bottom-gate, bottom-contact (BC) n-channel OTFTs examined with device simulation.

Table 1
Physical and structural parameters used for device simulation.

L (channel length)	10 μm
G (gate electrode length)	12 μm
W (channel width)	1 mm
S_t, D_t (thickness of source and drain electrode)	25 nm
T_{ox} (thickness of gate insulator (SiO_2))	300 nm
ε_{ox} (dielectric constant of gate insulator (SiO_2))	3.9
μ (electron mobility of semiconductor (n) layer)	0.5 $cm^2/(Vs)$
m^*(effective electron mass of semiconductor)	$1.15m_0$
ϕ_B (Schottky barrier height)	0.75–1.35 eV
E_g (band gap of semiconductor)	2.0 eV
T_S (thickness of n layer)	50 nm
ε_s (dielectric constant of organic semiconductor)	3.0
n (impurity concentration of n layer)	1×10^{16} cm^{-3}
T_{n+} (thickness of n^+ region)	10 nm
n^+(impurity concentration of n^+ region)	$1 \times 10^{16} - 1 \times 10^{20}$ cm^{-3}
Source voltage, V_S	0
Drain voltage, V_D	0–25 V
Gate voltage, V_G	0–25 V