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Design and modeling of self-aligned nano-imprinted sub-micrometer pentacene-based organic thin-film transistors

F. Zanella [a,h,*], N. Marjanović [a], R. Ferrini [a], H. Gold [b], A. Haase [b], A. Fian [b], B. Stadlober [b], R. Müller [c], J. Genoe [c], H. Hirshy [d], A. Drost [e], M. König [e], K.-D. Lee [f], J. Ring [f], R. Prétôt [g], C.C. Enz [h], J.-M. Sallese [h]

[a] CSEM Muttenz, Tramstrasse 99, 4132 Muttenz, Switzerland
[b] Institute of Nanostructured Materials and Photonics, Joanneum Research GmbH, Franz-Pichlerstrasse 30, 8160 Weiz, Austria
[c] imec, Kapeldreef 75, B-3001 Heverlee, Belgium
[d] Institute of Mechanical and Manufacturing Engineering, Cardiff University, Cardiff CF24 3AA, Wales, UK
[e] Fraunhofer EMFT, Hansastrasse 27 d, 80686 München, Germany
[f] Obducat Technologies AB, Scheelevägen 2, SE-223 63 Lund, Sweden
[g] BASF Schweiz AG, Areal Rosental, Schwarzwaldallee 215, 4057 Basel, Switzerland
[h] Swiss Federal Institute of Technology, EPFL, Station 11, 1015 Lausanne, Switzerland

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ABSTRACT

Sub-micrometer channel length (0.5 μm) organic thin-film transistors (OTFTs) are demonstrated using a process flow combining nano-imprint lithography (NIL) and self-alignment (SA). A dedicated test structure was designed and samples were fabricated on 4-in. plastic foils using a p-type sublimated small molecule (pentacene) as semiconductor. Field-effect mobilities, in saturation, between 0.1 and 1 cm^2/Vs were obtained not only for the supermicron OTFTs but also for the submicron OTFTs. Those devices were used to select a model based on the "TFT Generic Charge Drift model" which works well for a broad range of channel lengths including the submicron OTFTs. We show that these OTFTs can be accurately modeled, thus giving access to complex circuit simulations and design.

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1. Introduction

Organic thin-film transistors (OTFTs) allow producing low-cost and flexible circuits through the combination of low temperature processing – thus compatible with flexible substrates – and high-throughput fabrication techniques such as printing or vacuum sublimation applied in a roll-to-roll manner. Apart from the semiconductor/technology used, the trend in design is to scale down the transistor features to increase the speed as well as the integration level enabling more complex circuits and applications. In this paper we demonstrate the use of a technology based on UV-nano-imprint lithography (UV-NIL) and self-alignment (SA) [1] – which produces OTFTs with channel length (L) down to 0.5 μm and low gate/source–drain overlaps thus reducing the overlap parasitic capacitance – and we show that these OTFTs can be accurately modeled, thus giving access to complex circuit simulations and design. In the following sections, the complete workflow from the transistor layout to the modeling of the OTFTs is described.

2. Device fabrication

As gate electrode, aluminum is thermally evaporated onto a 4-in. plastic foil. A sacrificial layer and a UV-NIL resist are applied by spin coating. A 4-in. nickel shim is used

* Corresponding author at: CSEM Muttenz, Tramstrasse 99, 4132 Muttenz, Switzerland. Tel.: +41 61 690 6038; fax: +41 61 690 6000.
E-mail address: frederic.zanella@csem.ch (F. Zanella).

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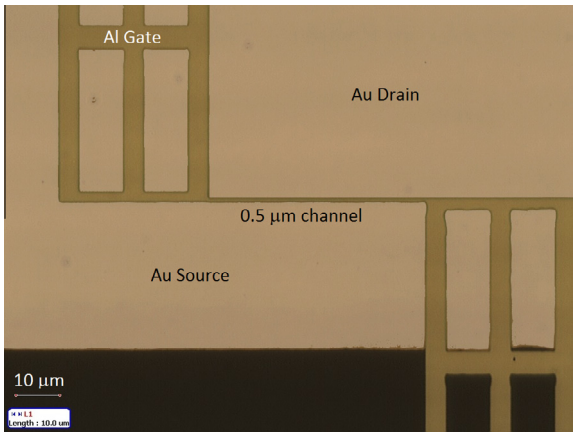

Fig. 1. Microphotograph showing the channel of a SA-NIL OTFT with $W/L = 50\ \mu m/0.5\ \mu m$.

as a template for intermediate polymer stamp, which in turn is used for the UV-NIL step to define the gate structure. After etch of the imprinted residual layer and of the aluminum, the double resist layer is stripped in a solvent. The dielectric is formed applying proprietary BASF material by spin-coating and subsequent UV-curing in ambient atmosphere. The dielectric is structured by photolithography with transfer of the structure through O_2 dry-etching. The devices reported in this paper have a nominal dielectric thickness of 200 nm and an averaged dielectric capacitance $C_i = 17\ nF/cm^2$. Source–drain (S/D) metal contact is structured with self-aligned photolithography. The details about the device fabrication will be published elsewhere.

Prior pentacene evaporation by organic molecular beam deposition (without further patterning, $t_{Pentacene} = 30$ nm), surface modification of the gold source–drains contact was performed by means of a heptadecafluoro-1-decanethiol based self-assembled monolayer, while surface modification of the dielectric was realized by a 10 nm poly (alpha-methylstyrene) (PαMS) layer [2] (neglected in C_i).

3. Layout design

A 2×2 array test layout compatible with this specific fabrication method was designed for modeling purpose. Each $28 \times 25\ mm^2$ quadrant comprises OTFTs, one is depicted in Fig. 1, inverters, capacitors (Self-Aligned-NIL compliant design), ring-oscillators and other test structures.

Dummy structures were added uniformly in the design on the NIL area in order to prevent undesired resist displacement resulting in ghost features and ease the lift-off process.

4. Results

The OTFTs were measured in inert atmosphere with an Agilent 4156C. The output and transfer characteristics of several submicron OTFTs are plotted in Fig. 2.

Transistors exhibited typical p-type enhanced mode behaviour when negatively biased, with field-effect mobility, extracted in the saturation regime (μ_{sat}), in the order of $10^{-1}\ cm^2/Vs$. Whereas such values are common for large channel lengths (e.g. 10 µm and beyond) they are exceptional for channel lengths in the (sub) micrometer range, indicating good charge injection from S/D contacts into the semiconductor [3]. The mobility μ_{sat} and corresponding threshold voltage, $V_{T,sat}$, are respectively displayed versus the channel length in Fig. 3(a and b) for a selected set of OTFTs. We report average values and standard deviations

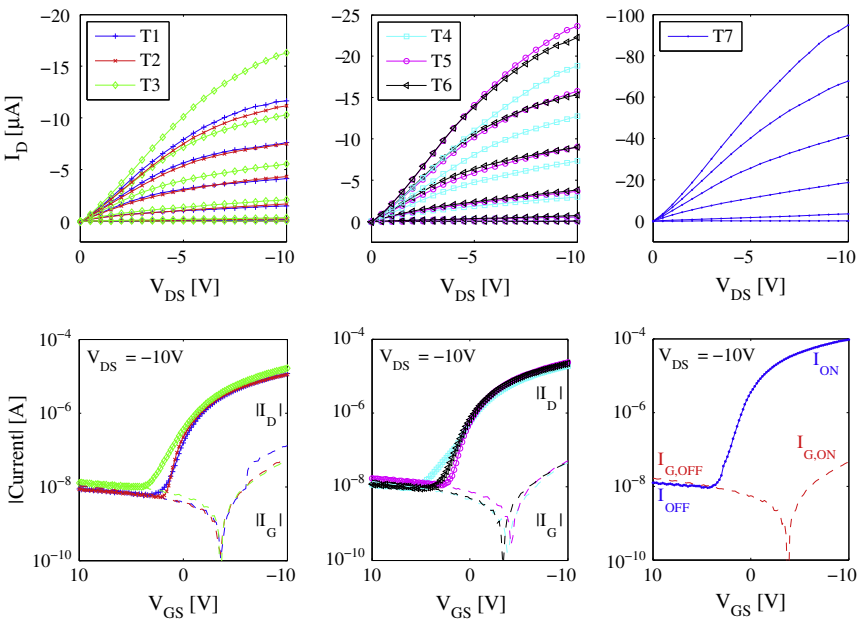

Fig. 2. Output (top) and transfer (bottom, in logarithmic scale) characteristics of submicron OTFTs with $L = 0.5\ \mu m$ and $W = 25\ \mu m$ (left), $W = 50\ \mu m$ (center) and $W = 250\ \mu m$ (right). *Note*: for all output curves in this paper: $5\ V \geqslant V_{GS} \geqslant -10\ V$, step $-2.5\ V$.

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