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High-performance pentacene thin-film transistor with ZrLaO gate dielectric passivated by fluorine incorporation

Chuan Yu Han [a], Ling Xuan Qian [a], Cheung Hoi Leung [a], Chi Ming Che [b], P.T. Lai [a,*]

[a] Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong
[b] Department of Chemistry, The University of Hong Kong, Hong Kong

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ABSTRACT

Pentacene thin-film transistor with high-κ ZrLaO gate dielectric has been fabricated for the first time. After treating the dielectric in a fluorine plasma, the carrier mobility of the transistor can be greatly improved to 0.717 cm^2/V s, which is more than 40 times that of one without plasma treatment. The major reasons should be larger pentacene grains and fewer traps in the device with gate dielectric passivated by the fluorine plasma. AFM confirms that relatively large and high pentacene islands form on the plasma-treated dielectrics in the initial growth stage, and the growth pattern obviously follows the Vollmer–Weber growth model. Furthermore, the surfaces of the dielectrics with different plasma treatment times are investigated by AFM, XPS and contact-angle measurement to reveal the mechanism/effects of the fluorine incorporation. Lastly, after exposure to atmosphere without encapsulation for 6 months, all the devices still display good transistor characteristics.

1. Introduction

Organic thin-film transistors (OTFTs) have attracted considerable research interest due to their commercial opportunities, such as flexible display, large-area sensor and radio-frequency identification tags [1–3]. The operation and performance of an OTFT are highly dependent on the interface between its gate dielectric and organic material. To improve the carrier mobility of the OTFT, much attention has been paid to interface modification, including self-assembled monolayer [4], annealing [5] and plasma treatment. Among them, plasma treatment is efficient and convenient to improve the surface characteristics in surface engineering. Oxygen plasma [6,7], N_2O plasma [8] and fluorine plasma [9] have been reported to modify the dielectric surface and good results were obtained. Moreover, fluorine-based plasma has long been investigated to provide valuable surface properties in organic and inorganic material fields [10–14]. Generally, the operating voltage of OTFTs based on SiO_2 gate dielectric is very high. Avoiding this drawback by reducing the thickness of the gate dielectric inevitably leads to large gate leakage current. Therefore, high-κ dielectric used as the insulator layer is a better alternative to lower the threshold voltage, and also thin the device to make it more flexible [15].

In this study, high-κ ZrLaO is proposed as the gate dielectric for pentacene OTFT, and is treated in fluorine plasma for surface modification. With appropriate plasma treatment time, the OTFT can achieve high performance, e.g. high carrier mobility as well as small threshold voltage. Moreover, after 6-month exposure to atmosphere, the devices can still show good transistor characteristics.

2. Experimental details

Pentacene OTFTs were fabricated by employing the bottom-gate top-contact configuration. Heavily-doped silicon wafers (n-type, ⟨100⟩, resistivity of 0.5–0.7 Ω cm) were cleaned according to the standard RCA method and dipped

* Corresponding author. Address: Room 505, CYC Building, Pokfulam Road, The University of Hong Kong, Hong Kong. Tel.: +852 28592691.
E-mail address: laip@eee.hku.hk (P.T. Lai).

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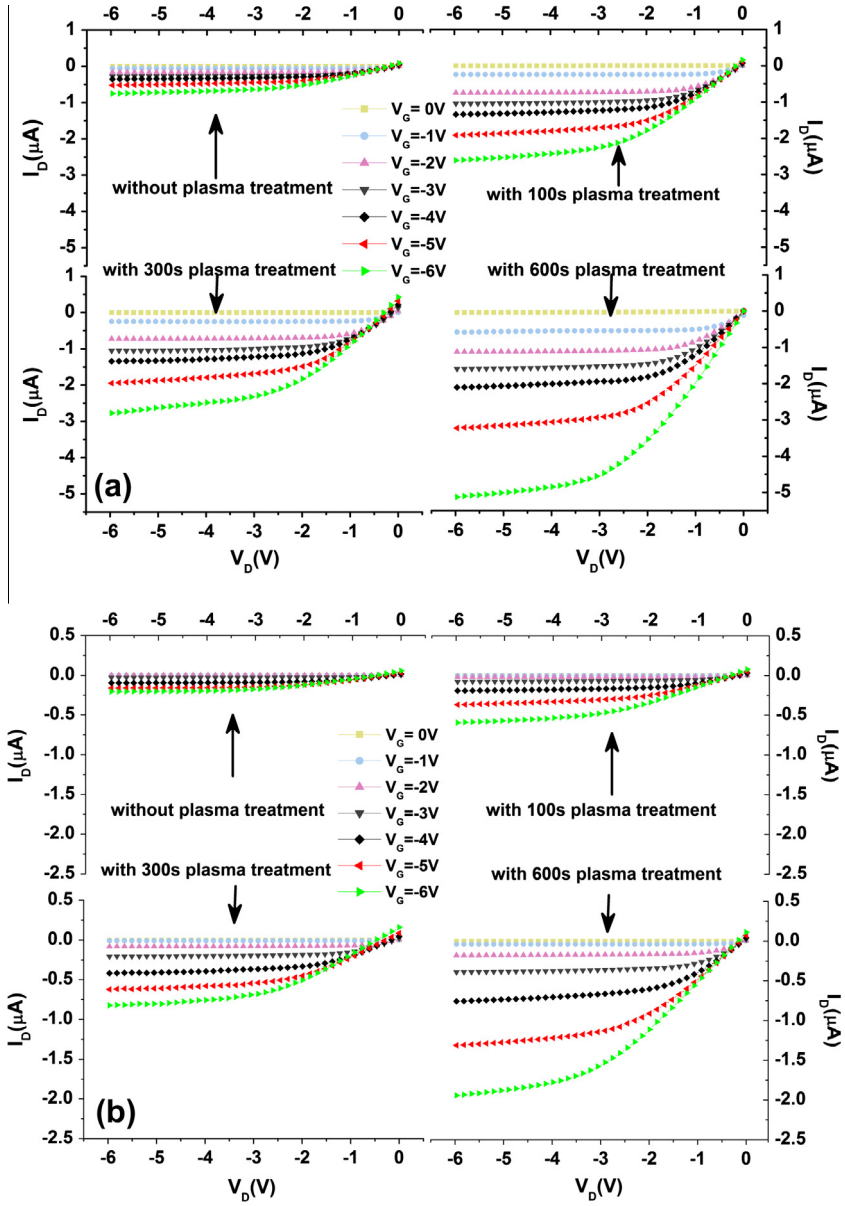

Fig. 1. Output characteristics of the OTFTs with different plasma treatment times: (a) fresh and (b) after 6 months.

in dilute HF acid (2%) to remove the native oxide. Next, ZrLaO insulator layer was sputtered at room temperature by radio-frequency sputterer (Denton Vacuum LLC Discovery 635). Then, the dielectric was annealed at 400 °C in NH_3, at a flow rate of 1000 mL/min for 10 min. After that, the samples were divided into four groups, which were treated in a fluorine plasma, at a flow rate of 10 sccm for CHF_3 and 1 sccm for O_2, for different durations of 0 s, 100 s, 300 s and 600 s. Then, 30-nm or 3-nm pentacene (p-type organic semiconductor, 99% purity, purchased from Sigma–Aldrich without purification) was evaporated on the dielectrics by an evaporator (Edwards Auto 306). The films were evaporated in high vacuum (5×10^{-6} torr) on the dielectrics at a deposition rate of 1.2 nm/min, monitored by a quartz-crystal oscillator. Lastly, drain and source electrodes were deposited on the 30-nm pentacene films by gold evaporation through a shadow mask to form the OTFTs. The width and length of the channel on the shadow mask were 200 μm and 30 μm, respectively. On the other hand, the 3-nm (about 2 monolayers) pentacene films were used to study their growth mechanism in the initial stage.

The *I–V* characteristics of the transistors were measured by an HP 4145B semiconductor parameter analyzer. The measurements were repeated after the samples were stored in atmosphere without encapsulation for 6 months. Al/ZrLaO/heavily-doped Si structure was used to fabricate capacitors by lithography for measuring the dielectric