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Letter

Teflon/SiO_2 bilayer passivation for improving the electrical reliability of pentacene-based organic thin-film transistors

Ching-Lin Fan [a,b,*], Yu-Zuo Lin [a], Ping-Cheng Chiu [a], Shea-Jue Wang [c], Win-Der Lee [d]

[a] Department of Electronic and Computer Engineering, National Taiwan University of Science and Technology, No. 43, Sec. 4, Keelung Rd., Da'an Dist., Taipei City 106, Taiwan
[b] Graduate Institute of Electro-Optical Engineering, National Taiwan University of Science and Technology, No. 43, Sec. 4, Keelung Rd., Da'an Dist., Taipei City 106, Taiwan
[c] Institute of Materials Science and Engineering, National Taipei University of Technology, No. 1, Sec. 3, Chung-Hsiao E. Rd., Da'an Dist., Taipei City 106, Taiwan
[d] Department of Electrical Engineering, Lee-Ming Institute of Technology, No. 2-2, Lee-Zhuan Rd., Taishan Dist., New Taipei City 243, Taiwan

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ABSTRACT

We demonstrate a bilayer passivation method using a Teflon and SiO_2 combination layer to improve the electrical reliability of pentacene-based organic thin-film transistors (OTFTs). The Teflon was deposited as a buffer layer using a thermal evaporator that exhibited good compatibility with the underlying pentacene channel layer, and can effectively protect the OTFTs from plasma damage during the SiO_2 deposition process, resulting in a negligible initial performance drop in OTFTs. Furthermore, because of the excellent moisture barrier ability of SiO_2, the OTFTs exhibited good time-dependent electrical performance, even after 168 h of aging in ambient air with 60–80% relative humidity.

1. Introduction

Organic thin-film transistors (OTFTs) have recently attracted considerable attention because of their low-temperature and low-cost fabrication process [1–3], which makes them suitable for large-area and low-cost flexible electronics. However, when the OTFTs are operated in ambient air, they tend to degrade easily because the organic semiconductor is very susceptible to moisture [4,5]. Therefore, the passivation of OTFT is necessary to elongate its lifetime by protecting the organic semiconductor from ambient air. Generally, silicon dioxide (SiO_2) is one of the most widely used passivation materials in solid-state electronic and optoelectronic devices because of its excellent oxygen and moisture barrier performance [6]. Moreover, the SiO_2 deposition has the compatibility with normal manufacturing processes for large-area deposition, such as plasma-enhanced chemical vapor deposition (PECVD) or radio-frequency (RF) sputtering. However, the deposition techniques are based on plasma process which is harmful to organic materials [7]. Therefore, an appropriate buffer layer between organic semiconductor and SiO_2 passivation layer is necessary to protect the OTFTs from plasma damage during the SiO_2 deposition process; furthermore, the processes and materials used in buffer layer deposition must be compatible with the underlying organic semiconductor to not degrade the device performance. Some previous research used solution-processed polymer, such as water-soluble polyvinyl alcohol (PVA), as the buffer layer in contact with the organic semiconductor for OTFTs because it causes less damage to the organic semiconductor compared to other polymers dissolved in

* Corresponding author at: Department of Electronic and Computer Engineering, National Taiwan University of Science and Technology, No. 43, Sec. 4, Keelung Rd., Da'an Dist., Taipei City 106, Taiwan. Tel.: +886 2 27376374; fax: +886 2 27376424.
E-mail address: clfan@mail.ntust.edu.tw (C.-L. Fan).

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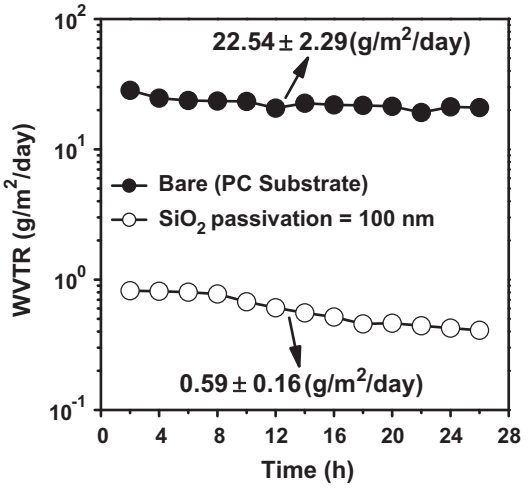

Fig. 1. WVTR of PC substrates with and without a 100-nm-thick SiO_2.

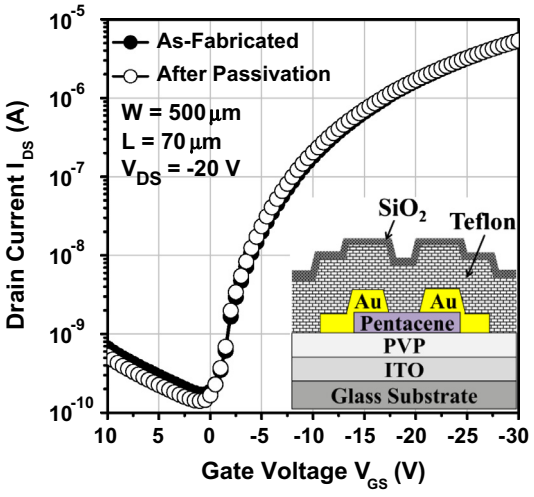

Fig. 2. Transfer curves (I_{DS}–V_{GS}) of the OTFTs before and after Teflon/SiO_2 passivation (the inset image is the schematic diagram of an OTFT with Teflon/SiO_2 passivation).

organic solvents [5,8]. However, there is still a large initial performance drop in OTFTs after PVA passivation [5,9,10], which might be attributed to the chemical or structural changes that occur for the organic semiconductor after a reaction with the PVA solution. Therefore, a solvent-free or completely dry process is preferred to prepare the buffer layer for OTFTs. Considering these requirements, thermally evaporated organic materials may be a strong candidate for buffer layer application because of their flexibility and compatibility with the underlying organic semiconductor.

Polytetrafluoroethylene (Teflon) is known as a non-polar polymer with many excellent properties, such as gas and moisture barriers, chemical resistance, thermal resistance, and electric insulation. Teflon can be readily deposited using a thermal evaporator with low-evaporation temperature to not damage the underlying organic semiconductor by thermal stress during the evaporation process [11,12]. Therefore, we presume that using thermally evaporated Teflon as a buffer layer will have good compatibility with the underlying organic semiconductor, and can protect the OTFTs form plasma damage during the SiO_2 deposition process. Furthermore, Teflon has been reported as a single passivation layer to improve the electrical reliability of OTFTs [13,14]. However, these reported schemes for obtaining a Teflon layer are based on a plasma process, which may cause plasma damage to the underlying organic semiconductor, resulting in a large initial performance drop in OTFTs. In a recent report, Scharnberg et al. have proposed thermally evaporated Teflon as an electret passivation layer for pentacene-based OTFTs [15]. Although the passivation with corona-charged Teflon favorably controls the threshold voltage, it causes a large decrease in the on/off current ratio and carrier mobility. Therefore, this study introduces the use of non-charged Teflon as a buffer layer, and combines it with SiO_2 barrier layer to serve as bilayer passivation for the OTFTs. It was found that there was no noticeable initial performance drop in OTFTs after Teflon/SiO_2 passivation, implying that thermally evaporated Teflon did not cause damage to the underlying pentacene layer, and can effectively protect the OTFTs from plasma damage during the SiO_2 deposition process. Furthermore, the moisture effect on the reliability of the OTFTs was greatly reduced after Teflon/SiO_2 passivation because of the decreased water vapor transmission rate (WVTR). It is believed that the proposed bilayer passivation with combination of Teflon and SiO_2 can be successfully applied to OTFT passivation to improve the electrical reliability.

2. Experiment

The pentacene-based OTFTs with top-contact structure were used in this study. A glass substrate with an indium-tin-oxide (ITO) layer was used as a substrate and as a bottom gate electrode. A 600-nm-thick cross-linked poly(4-vinylphenol) (PVP) was coated as a gate dielectric on the ITO layer using two-step spin coating, and cured in vacuum oven at 180 °C for 1 h. A 50-nm-thick pentacene was then deposited as a channel layer on the PVP layer by a thermal evaporator (base pressure of 2×10^{-6} Torr) at a deposition rate of 0.2 Å/s with the substrate temperature maintained at room temperature (RT). Gold (50 nm) source/drain contacts (width = 500 μm and length = 70 μm) were deposited through a shadow mask on the pentacene channel layer by a thermal evaporator (base pressure of 2×10^{-6} Torr). Finally, the passivation layer, composed of Teflon and SiO_2, was deposited over the OTFTs. Teflon (400 nm) was deposited by a thermal evaporator (base pressure of 2×10^{-6} Torr) with the substrate temperature maintained at RT. SiO_2 (100 nm) was deposited by RF magnetron sputtering using a SiO_2 target under the parameters of 50 W and 3.5 m Torr at RT. All devices were measured under ambient conditions (i.e., RT and 60–80% relative humidity (RH)) using a semiconductor parameter analyzer (HP 4145B).

3. Results and discussion

To confirm the moisture-blocking ability of sputtered SiO_2 film, the WVTR of 100-nm-thick SiO_2 deposited on