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Letter

Solution-processed single-crystalline organic transistors on patterned ultrathin gate insulators

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ABSTRACT

Single-crystalline organic transistors of 3,11-didecyl-dinaphtho[2,3-*d*:2′,3′-*d*′]benzo[1,2-*b*:4,5-*b*′]dithiophene (C_{10}-DNBDT-NW) and 2,9-didecyl-dinaphtho[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene (C_{10}-DNTT) were fabricated by solution processes on top of the patterned hybrid ultrathin gate dielectrics consisting of 3.6 nm-thick aluminum oxide and self-assembled monolayers (SAMs). Due to the excellent crystallinity of the channel films, bottom-gate and top-contact field-effect transistors exhibited the average field-effect mobility of 3.7 $cm^2/V\,s$ and 4.3 $cm^2/V\,s$ for C_{10}-DNBDT-NW and C_{10}-DNTT, respectively. These are the first successful devices of solution-processed single-crystalline transistors on ultrathin gate dielectrics with the mobility above 1 $cm^2/V\,s$, opening the way to develop low-power-consumption and high-performance printed circuits.

1. Introduction

The development of organic thin-film transistors (OTFTs) has attracted great interest for next-generation flexible devices such as electric papers and conformable sensor arrays [1]. In particular, the reports about high-mobility OTFTs beyond 10 $cm^2/V\,s$ [2–4] raised the expectation for the application of the organic semiconductors to high-speed logic circuits such as radio-frequency identification tags, flexible display drivers and wearable computers [5]. A straightforward approach to realizing high-performance OTFTs is to use single-crystalline organic semiconductor channels, since the grain boundaries are known to reduce carrier mobility significantly as well as device stability and reproducibility. Several groups have already succeeded to fabricate quite large crystalline domains of organic semiconductors by solution processes, and all these OTFTs exhibited considerably high mobilities [3,6,7]. However, the application of these methods has been limited so far to the preliminary devices where the crystals were grown on the smooth and homogeneous surface of SiO_2/Si wafers. In order to realize logic circuits and active matrix for displays, the single-crystalline films need to be formed on top of substrates with patterned gate electrodes while the inhomogeneous surface energy, topography and/or morphology of the substrates may cause random nucleation of crystals. Thus it is a challenging issue to form single-crystalline films on top of the patterned substrates by suppressing the undesirable nucleation of crystals.

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Edge casting is one of the methods to grow large crystalline domains of organic semiconductor films from a small amount of solution [6]. The method uses a solution-holding piece on substrates in order to control the drying direction of the solution. Because the crystal nucleation occurs only at one side of the solution droplet, inch-size crystal domains along the crystal growth direction can be obtained [8]. One unique feature of edge cast is that the crystallization occurs at the liquid/air interface slightly above the contact line; Thus, it is expected that the nucleation of crystals should not be affected as much as other solution methods. It is also important to combine this method with the ultrathin gate insulators consisting of a few nm of aluminum oxide and self-assembly monolayers (SAMs) [9–12], since the reduction of operation voltage down to a few volts should be essential for realizing mobile devices driven by batteries or wireless power sources [13].

In this paper, we demonstrate the solution process of single-crystalline OTFTs on top of a variety of ultrathin gate dielectrics. High performances were successfully obtained with two kinds of organic semiconductors, 3,11-didecyldinaphtho[2,3-*d*:2′,3′-*d*′]benzo[1,2-*b*:4,5-*b*′]dithiophene (C_{10}-DNBDT-NW, Fig. 1(a)) [8] and 2,9-didecyl-dinaphtho[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene (C_{10}-DNTT, Fig. 1(b)) [14], and with four kinds of gate dielectrics by edge cast method. The highest mobility of 5.2 $cm^2/V\,s$ was achieved at the small gate voltage of 2 V for the combination of C_{10}-DNTT and AlO_x without SAM. The variation in device properties is also discussed in terms of the film crystallinity and the surface property of gate insulators.

2. Experimental

Aluminum gate electrode was deposited on silicon/thermal silicon oxide (500 nm) substrate by thermal evaporation under 10^{-7} mbar through a shadow mask [4]. Approximately 3.6 nm of aluminum oxide was formed by O_2 plasma to fabricate hybrid dielectric. The substrates were then immersed in the 2-propanol solutions of SAMs about 24 h: 0.2 mM 16-phosphonohexadecanoic acid (PHDA, Fig. 1(c)), 0.05 mM 11-hydroxyundecylphosphonic acid (HO–C_{11}–PA, Fig. 1(d)), 0.1 mM phenylphosphonic acid (PhPA, Fig. 1(e)), 0.05 mM tetradecylphosphonic acid (C_{14}–PA, Fig. 1(f)), and 0.05 mM 12,12,13,13,14,14,15,15,16,16,17,17,18,18,18H-pentadecafluoro-octadecyl phosphonic acid ($F_{15}C_{18}$–PA, Fig. 1(g)) [11]. The bare aluminum oxide gate insulator was also used for comparison. The capacitances were measured at 0.88 $\mu F/cm^2$ for PHDA, 0.75 $\mu F/cm^2$ for HO–C_{11}–PA, 1.1 $\mu F/cm^2$ for PhPA and 1.27 $\mu F/cm^2$ for bare AlO_x, which were measured with the Au/insulator/Al structure of 50 × 50 μm in size.

We used C_{10}-DNBDT-NW and C_{10}-DNTT as channel materials. The single crystals of the organic semiconductors were grown on the hybrid dielectrics by the edge-cast method [15] as shown in Fig. 2(a). C_{10}-DNBDT-NW and C_{10}-DNTT were dissolved in 1,2-dimethoxybenzene at 0.07 wt% and in tetralin at 0.05 wt%, respectively. Then the solution was dropped near the edge of a glass piece which was placed on the substrate to hold the solution [16]. As the solvent evaporated, the edge of the droplet shifted toward the glass piece so that the direction of the crystal growth is perpendicular to the edge of the glass piece. The processes were carried out on a hot plate kept at 125 °C for C_{10}-DNBDT-NW and at 100 °C for C_{10}-DNTT. After the crystal growth, the films were annealed in vacuum oven at 100 °C under the pressure of 10 mbar in order to remove the remaining solvent. The thickness of the semiconductor films was estimated at 10–30 nm by atomic force microscopy (AFM). Finally, 30 nm-thick gold electrodes for source and drain were thermally evaporated in vacuum through shadow masks. The channel length was designed to be 20–300 μm, and the channel width 500 μm. The device performance was measured in air by semiconductor device analyzer (B1500A, Agilent).

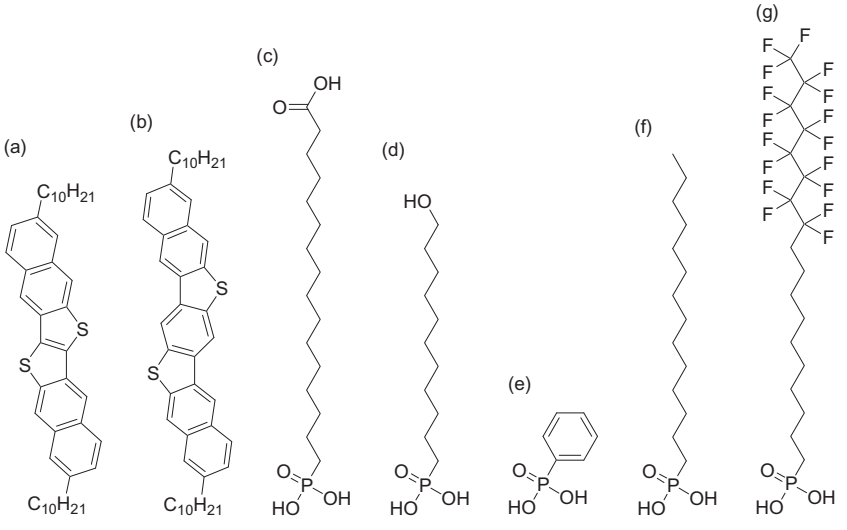

Fig. 1. Molecular structures of (a) C_{10}-DNTT, (b) C_{10}-DNBDT-NW, (c) PHDA, (d) HO–C_{11}–PA, (e) PhPA, (f) C_{14}–PA, and (g) $F_{15}C_{18}$–PA.

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