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Scaling down of organic complementary logic gates for compact logic on foil

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ABSTRACT

In this work, we realize complementary circuits with organic p-type and n-type transistor integrated on polyethylene naphthalate (PEN) foil. We employ evaporated p-type and n-type organic semiconductors spaced side by side in bottom-contact bottom-gate coplanar structures with channel lengths of 5 μm. The area density is 0.08 mm^2 per complementary logic gate. Both p-type and n-type transistors show mobilities >0.1 $cm^2/V\,s$ with V_{on} close to zero volt. Small circuits like inverters and 19-stage ring oscillators (RO) are fabricated to study the static and the dynamic performance of the logic inverter gate. The circuits operate at V_{dd} as low as 2.5 V and the inverter stage delay at V_{dd} = 10 V is as low as 2 μs. Finally, an 8 bit organic complementary transponder chip with data rate up to 2.7 k bits/s is fabricated on foil by successfully integrating 358 transistors.

1. Introduction

In recent years, ever more complex organic integrated circuits on foil have been demonstrated ranging from RFID tags to a microprocessor. Nearly all those circuits have been realized in unipolar logic [1,2]. In order to realize circuits with higher integration levels, complementary circuits are preferred for their large noise margin, low static power dissipation, and potentially higher operation speed compared to unipolar circuits.

Various efforts have been made to realize organic complementary logic. Small logic units, such as inverter with ultralow operation voltages [3] and ring oscillator with high oscillation frequencies [4] have been realized in organic complementary technologies. Crone et al. have realized organic complementary 48-stages shift registers by evaporating organic semiconductors with a coarse shadow mask on a substrate with coplanar TFT structures [5]. Klauk et al. and Someya et al. fabricated organic complementary circuits with inverted staggered structures by evaporating organic materials and metal layers through ultra-fine shadow masks with a precise mask alignment system in vacuum. Logic on foil with few hundreds TFTs have been realized in this way [6,7]. Realizing organic complementary circuits by direct ink-jet printing (IJP) of the organic active layers on defined p-type and n-type regions is also reported [8–14]. Small circuits with a complexity up to a three bit decoder for memory readout [11] have been realized.

Nonetheless, a major issue that limits the integration level of organic complementary circuits is the area consumption per logic gate. Here the challenge is not only

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the size of the p-type and n-type semiconductor areas that need to be accurately defined, but also the tight spacing between the p-type and n-type transistors. Using previously published design rules for organic complementary circuits results in huge die sizes for complex circuits like RFID tags or line-drivers. This limits the yield and increases the cost of those organic complementary circuit technologies.

To realize a high level of integration, photolithography is widely used in the semiconductor industry to pattern different layers of material. Patterning organic semiconductors by photolithography to fabricate unipolar organic integrated circuits [1,2,15] has been demonstrated before. The difficulty for organic complementary circuits is to implement photolithography to pattern both p-type and n-type semiconductor side by side with high yield. The patterning of the second organic semiconductor layer degrades the first fabricated TFTs due to the fragility of the organic semiconductor.

Here, we realize fully integrated organic complementary circuits on polyethylene naphthalate (PEN) foil by using evaporated p-type and n-type organic semiconductors. Besides the thermal evaporation of p-type and n-type organic semiconductors, all processes are done in ambient air condition. The p-type and n-type organic active layers are patterned by photolithography, resulting in a high area density of 0.08 mm^2 per complementary logic gate. The processes are similar to those used in the current flat panel display (FPD) industry. Both p-type and n-type transistors show mobilities >0.1 $cm^2/V\,s$ with V_{on} close to zero volt in bottom-contact bottom-gate coplanar structures with channel lengths of 5 μm. Small circuits like inverters and 19-stage ring oscillators (RO) are fabricated to study the static and the dynamic performance of the logic inverter gate. The inverter stage delay at V_{dd} = 10 V is as low as 2 μsec. Finally, an 8 bit organic complementary transponder chip is fabricated on foil by successfully integrating 358 transistors. The latter indicates a good yield and robustness of the process flow and is encouraging for the future of organic electronics in flexible electronic applications.

2. Foil-on-carrier substrate fabrication

In this work, we use a foil-on-carrier (FOC) approach and process on a 6″ wafer to realize the organic complementary integration. PEN foil of 25 μm thick is laminated on a silicon wafer. We fabricate a patterned gate electrode, gate insulator and source–drain electrode (S–D) layers, respectively, by conventional photolithography. As a result, a metal-insulator-metal (MIM) stack is prepared, ready for the following organic semiconductor process. The schematic image of the FOC substrate and a picture of the 6-in. FOC substrate with MIM structure is shown in Fig. 1a and c. Thirty nm of Ti–Au is used as S–D metal and 100 nm of Al_2O_3 is used as insulator layer. A microscope image of the inverter is shown in Fig. 1b. The p-type and n-type TFTs are placed side-by-side separated by a distance of 80 μm. The area per complementary inverter is consequently around 0.08 mm^2, which allows us to implement many advanced circuits on one substrate.

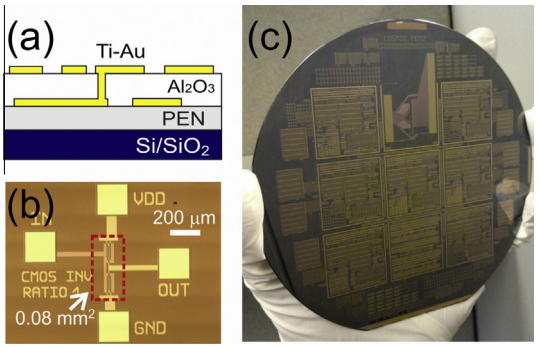

Fig. 1. (a) The schematic cross-section of the metal-insulator-metal stack on foil-on-carrier substrate. (b) Microscope image of a complementary inverter, the size per inverter is 0.08 mm^2. (c) The photograph of the 6-in. foil on carrier substrate.

3. Properties of discrete OTFTs

To benefit from the advantages of complementary logic, there are some requirements for the integrated TFT characteristics. First, the current levels of the p and n-type transistors in an inverter, driven at V_{dd} and V_{gnd}, need to be matched in order to maximize the noise margins. Second, the turn-on voltages need to be very close to zero in order to minimize the leakage currents in the static states of the complementary inverter. Third, to obtain high operation speeds, the current drive of the TFTs has to be maximized. To reduce parasitic overlap capacitances, high mobilities of both p-type and n-type semiconductors are preferred, rather than large W/L ratios in order to obtain high current drive. In order to obtain the desired TFT characteristics in a coplanar structure, specific processes for p-type and n-type TFTs are developed on the discrete transistor level first. For the p-type TFTs, substrates with coplanar structures are treated by pentafluorobenzenethiol (PFBT) in order to form a self-assembled monolayer (SAM) on the gold bottom contacts. Afterwards, a layer of poly(α-methylstyrene) (PαMS) is spin-coated on the substrate. Since the solution is repelled from the fluorinated thiol covered source/drain contacts, only the dielectric is passivated by this thin polymer layer [16]. In this work, 3,9-diphenyl-*peri*-xanthenoxanthene (Ph-PXX) [17], synthesized in-house and purified by thermal gradient sublimation, is employed as p-type semiconductor because of its high thermal and chemical stability in TFT structures. The p-type TFTs are hence perfectly suited to be processed first in the complementary integration flow. Thirty nm of Ph-PXX is evaporated on the substrate at a substrate temperature at 68 °C and a deposition rate of 0.3 Å/s. The transfer characteristics of the p-type TFTs are shown in Fig. 2a. The electrical characteristics of the TFTs are measured in an inert environment to avoid interference of oxygen and moisture. The effective mobility (μ_{eff}) is calculated by Eq. (1), where W is the channel width, L is the channel length, I_d is the drain current, C_{ox} is the oxide capacitor, V_{gs} is the gate to source voltage, respectively:

$$\mu_{eff} = \frac{2L}{WC_{ox}}\left(\frac{d\sqrt{I_d}}{dV_{gs}}\right)^2 \quad (1)$$