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Ferroelectric random access memory based on one-transistor–one-capacitor structure for flexible electronics

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ABSTRACT

We have demonstrated a low temperature process for a ferroelectric non-volatile random access memory cell based on a one-transistor–one-capacitor (1T1C) structure for application in flexible electronics. The n-channel thin film transistors (TFTs) and ferroelectric capacitors (FeCaps) are fabricated using cadmium sulfide (CdS) as the semiconductor and poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] copolymer as the ferroelectric material, respectively. The maximum processing temperature for the TFTs is 100 °C and 120 °C for the FeCaps. The TFT shows excellent access control of the FeCap in the 1T1C memory cell, and the stored polarization signals are undisturbed when the TFT is off. The fabricated 1T1C memory cell was also evaluated in a FRAM circuit. The memory window on the bit line was demonstrated as 2.3 V, based on the 1T1C memory cell with a TFT having dimensions of 80 μm/5 μm (W/L) and a FeCap with an area of 0.2×10^{-3} cm^2 using a bit line capacitor of 1 nF pre-charged at 17.2 V. The 1T1C memory cell is fabricated using photolithographic processes, allowing the integration with other circuit components for flexible electronics systems.

1. Introduction

Interest in flexible electronics continues to grow. Some of the potential applications include flexible, bendable or stretchable displays [1], sensors [2,3], solar cells [4], radio frequency identification tags (RFIDs) [5,6] and non-volatile memories [2,7]. To be compatible with these applications, new devices, materials, and alternate fabrication technologies that meet the low temperature process requirements of inexpensive flexible substrates (~150 °C) are needed. Organic materials and low temperature deposited inorganic thin film materials are promising due to their mechanical flexibility, simple process requirements and enhanced device performance. Many of these materials can be processed using solution based methods such as spin coating and printing, which in principle, provide low fabrication cost and low temperature processing [8,9].

Non-volatile memory is an important IC component in electronics systems. It requires a robust fabrication process as well as good performance. For flexible electronics, many types of memory devices have been investigated [10]. In particular, there are two types of device architectures that are of much interest, floating gate (or charge trapping) and ferroelectric based memories. The former type of memory utilizes the change in threshold voltage in the transistor due to the stored or trapped charges to differentiate the "0" and "1" states. The associated high quality tunneling and trapping layers in this type of non-volatile memory typically requires higher temperature processing [11], which is incompatible with many plastic substrates. To reduce process temperature, organic based trapping layers have been used [12]. However, due to the low-k value and thickness of these layers, high voltage is required to inject the charges into the trapping layer (or floating gate).

On the other hand, ferroelectric non-volatile random access memory (FRAM) utilizes the remanent polarization of a ferroelectric material for data storage. The remanent polarization is the retained polarization after removing

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the electric field. If the applied electric field is higher than the coercive field of the ferroelectric material, the dipoles can be switched and aligned with the electric field, resulting in a spontaneous polarization. The two stable states of the remanent polarization in positive and negative directions can be used for memory states "0" and "1" [13]. In addition, FRAM has lower operation voltage, faster write speed, longer endurance and less fatigue effect, compared to the commonly used floating gate or charge trapping based memory [13].

Poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] copolymer is one of the most promising organic ferroelectric materials for flexible FRAM applications. It is compatible with low temperature solution-based processes, and is chemically stable [7,14–17]. The polarization of P(VDF-TrFE) originates from the large difference in electronegativity between the fluorine, carbon and hydrogen atoms [18]. The polarization reversal originates from the rotation of the carbon–fluorine (C–F) and carbon–hydrogen (C–H) covalent bonds along the two sides of the main polymer chain [19,20]. Many groups have reported on the P(VDF-TrFE) based ferroelectric field effect transistors (FeFETs) [7,16,21]. However, secondary effects such as charge trapping at the ferroelectric semiconductor interfaces, depolarization field, and gate leakage can potentially degrade the reliability of this one-transistor (1T) device [22].

The one-transistor–one-capacitor (1T1C) architecture is another memory cell structure used in FRAM arrays. In this architecture, ferroelectric capacitors (FeCaps) are used to store data and transistors are used to control the access to the FeCap [23]. The amount of switching charge on the FeCap can be detected as a change in the voltage on the bit line. An advantage of the capacitor-based FRAMs is that the secondary effects seen in ferroelectric transistors mentioned previously are reduced because the charges are stored in FeCaps, which are built by sandwiching a thin layer of ferroelectric film between two metal contacts. The FeCaps have better reliability and endurance [24,25]. Here, we describe a low temperature process for a FRAM memory cell based on the 1T1C structure. The 1T1C memory cell is fabricated using photolithographic processes and can be easily integrated with other circuit components for system-on-chip devices. The integrated TFT and FeCap show good performance and a large memory window is achieved for the 1T1C memory cell. It is demonstrated that, when properly fabricated, the 1T1C memory cell is a promising device for flexible non-volatile memory applications.

2. Experimental

The fabricated 1T1C memory cell integrates two parts: (1) a n-channel thin-film transistor (TFT) for access control, which uses cadmium sulfide (CdS) as the semiconductor material, and (2) a FeCap for data storage based on P(VDF-TrFE) ferroelectric copolymers (Fig. 1). The process is composed of three major steps.

First, the CdS TFT is fabricated (Fig. 1a–d). It starts with the deposition of 100 nm of Cr for the gate electrode using e-beam evaporation. Then the gate metal is patterned and 90 nm of hafnium oxide (HfO_2) is deposited as the gate

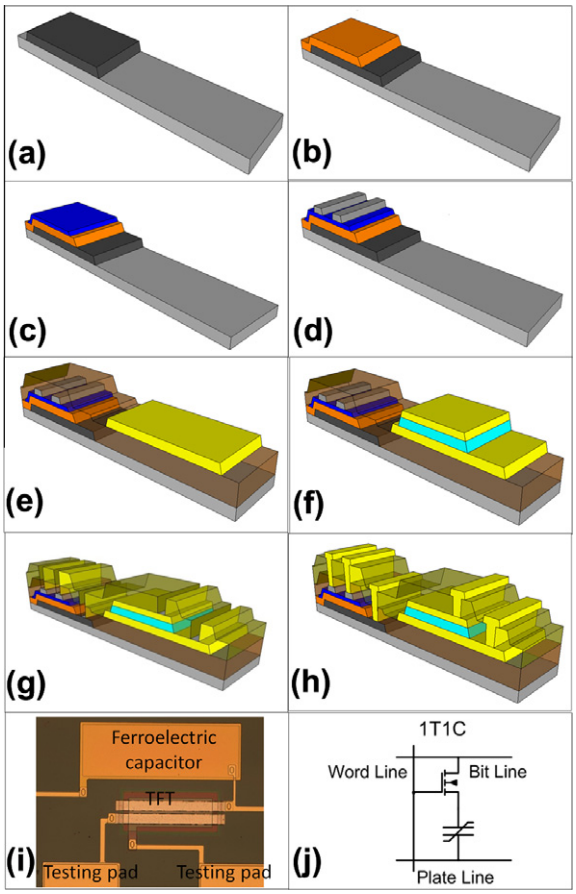

Fig. 1. (a–h) The fabrication process of the 1T1C device: the deposition and patterning of (a) Cr gate, (b) HfO_2 gate dielectric, (c) CdS semiconductor, (d) Al for source and drain contacts for TFT, and (e) deposition of ILD1, deposition and patterning of bottom contact of the FeCap, (f) deposition and patterning of P(VDF-TrFE) film and top contact of the FeCap, (g) deposition of ILD2 and patterning of both ILD1 and ILD2, (h) deposition and patterning of the top interconnection, (i) an image of a fabricated 1T1C device with W and L of the TFT as 160 and 5 μm and the size of the FeCap as 3×10^{-4} cm^2, and (j) circuit schematic of the 1T1C device.

dielectric. The HfO_2 layer is deposited using atomic layer deposition (ALD) at 100 °C. It is important to note that this is the highest temperature used in the TFT process. Next, 30 nm of CdS is deposited using chemical bath deposition (CBD) at 70 °C [26]. The CdS and the HfO_2 layers are patterned to isolate the active area for each transistor using a wet etching process [27]. Finally, 100 nm of Al for source and drain electrodes is deposited using e-beam evaporation. The resulting TFTs are capsulated with 500 nm of parylene as the interlayer dielectric (ILD1).

The next step is the fabrication of the FeCaps (Fig. 1e and f). P(VDF-TrFE) copolymer powder with 70/30 mol ratio (Hisense Electronics Co., China) was dissolved in 2-butanone (3 wt.%) without further purification. First, gold (100 nm) is e-beam evaporated on top of the parylene ILD1 layer and patterned for the bottom contacts of the FeCaps. Next, the P(VDF-TrFE) is deposited by spin coating, followed by annealing (~20 Torr) at 120 °C for 2 h. The