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Hybrid CMOS thin-film devices based on solution-processed CdS n-TFTs and TIPS-Pentacene p-TFTs

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ABSTRACT

Fabrication and characterization of integrated hybrid complementary metal oxide semiconductor devices (CMOS) using 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-PC) and cadmium sulfide (CdS) as the active layers deposited using solution based processes are demonstrated. The n- and p-type thin film transistors (TFTs), inverters, and NAND gate devices were fabricated using photolithography-based techniques. The hybrid CMOS technology demonstrated is compatible with large-area and mechanically flexible substrates given the low temperature processing (<100 °C) and scalable design. The integrated n- and p-type devices show saturation mobilities of 15 and 0.02 cm^2/V s, respectively. The inverters exhibited a DC gain of ≈52 V/V with full rail-to-rail switching. The NAND logic gates switch rail-to-rail with a transition point of $V_{DD}/2$.

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1. Introduction

Large area organic and inorganic based circuits are receiving significant attention because of the demand for low-cost, low-temperature processable TFTs to enable full circuit integration in large-area flexible circuits [1]. In particular, solution based organic and inorganic semiconductors offer several advantages over traditional deposition techniques. Some of these advantages include low temperature deposition and patterning over large areas with high materials utilization. The low processing temperature allows these devices to be integrated on inexpensive flexible substrates. Photolithographically defined devices provide for the fabrication of complex circuits, not possible with shadow mask defined devices [2–4]. Unpatterned blanket layers can increase leakage current and restrict access to vias to connect with other levels in an integrated circuit [5]. Shadow masks on the other hand prohibit patterning large areas with small features [1,6]. In this paper, we demonstrate scalable integrated processes and techniques that utilize standard photolithographic techniques that allow more complex device fabrication using solution-based semiconductors.

Solution processable semiconducting materials are attractive because they can be deposited using simple low temperature methods such as spin coating, dip coating, and ink-jet printing [7–9]. While n-type organic semiconductors have progressed, their performance still does not compete with n-type inorganic semiconductors [10,11]. The lack of stable, moderate performance n-type organic field effect transistors (OFETs), and the complexity of integrating p-type and n-type OTFTs in a photolithographic process has limited the development of all organic CMOS devices [9,12,13].

In this paper, we demonstrate a fully integrated approach to fabricate CdS/TIPS-PC CMOS digital logic circuits. The CMOS integration process includes six photolithography steps. In our approach, CdS is the n-type semiconductor and is deposited using chemical bath deposition (CBD) at

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70 °C. CBD is a low temperature process suitable for large area and flexible electronics that provides mobility values >10 cm^2/V s after full integration [14,15]. The p-type transistors are fabricated using a solution of TIPS-PC (30 mg/ml) dissolved in 1,2,3,4-tetrahydronaphthalene (Tetralin) with measured mobility values as high as 9×10^{-2} cm^2/V s with an average mobility of 2×10^{-2} cm^2/V s, after full integration. Threshold voltages after integration were 12 and −3.5 V, respectively. Our TIPS-PC performance is comparable to the performance reported for spin-on TIPS-PC OTFTs [16–18]. CdS performance is comparable to our original report for shadow mask CdS TFTs [15]. We also demonstrate a complementary inverter and a NAND gate that exhibit full rail-to-rail switching with a switching threshold voltage of 10 V, approximately half of the supply voltage. This work reports alternate integration as well as solution based processes for both n- and p-channel semiconductors with 6x increase in gain due to the higher I_{on}/I_{off} ratios achieved with the improved CMOS integration. Our previous report used vacuum-base processes for semiconductor deposition [14].

2. Experimental

Fig. 1 shows a schematic cross-sectional view of the full photolithographically defined hybrid solution-based inorganic/organic CMOS circuits. The devices are fabricated on a Si (100) substrate with a 500 nm layer of thermally grown SiO_2 for isolation between the substrate and the sample. First, 80 nm of chromium (Cr) is deposited using e-beam evaporation. The Cr layer is used for the n- and p-type gate, defined with a single mask. The Cr layer is wet etched with chromium etchant (CR-7, Cyantek Inc.). Next, the n-MOS TFT gate dielectric (90 nm of HfO_2 at 100 °C, 600 cycles) is deposited using atomic layer deposition (ALD). Tetrakis (ethylmethylamino) hafnium (TEMAH) and H_2O are used as precursors for HfO_2 growth. Following the gate dielectric deposition, an ammonia-free CBD process is used to deposit 60 nm of CdS on top of HfO_2 at 70 °C [15]. A hardmask layer of parylene-C (500 nm) is deposited by chemical vapor deposition (CVD) and Si_xN_y (12 nm) deposited using plasma enhanced chemical vapor deposition (PECVD) was used to protect the CdS layer during subsequent processing. The purpose for the hardmask is twofold; first to protect the CdS layer from being etched during the p-type device fabrication and secondly it facilitates wet etching the CdS (10:1 HCl) layer. The hardmask is patterned using an O_2/CF_4 reactive ion etch (RIE) (100 mTorr, 50 W) to first remove the Si_xN_y and then O_2 RIE (100 mTorr, 50 W) is used to etch the parylene-C inter layer dielectric (ILD). The CdS is patterned with a 1:10 HCl/water solution. The HfO_2 gate dielectric is etched separately with a buffered oxide etch (BOE 7:1, J.T. Baker). This step also opens a via to the p-type TFT gate metal. The p-type OTFT is fabricated next. A parylene-C (500 nm) ILD is deposited and etched using the same process as the ILD for the n-type TFT device. Parylene-C (150 nm) is deposited to form the gate dielectric layer for the p-type TFT. O_2 RIE (100 mTorr, 50 W, 100 nm/min) is used to pattern the parylene layers, and open vias to the contact pads. After opening the vias, Au (100 nm) is deposited by e-beam evaporation at 0.5 nm/min for the S–D contacts and interconnections to complete the CMOS integrated circuit. Finally, TIPS-PC (30 mg/ml, 200 nm) is deposited using spin casting (1500 rpm, 120 s) and baked at 60 °C for 20 min. Parylene-C is used as encapsulation. O_2/CF_4 RIE is used to etch the TIPS-PC, after the encapsulation layer has been etched with O_2 RIE. Patterned TIPS-PC shows a higher I_{on}/I_{off} ratio and low gate leakage as compared to unetched layers. We found that a small percentage of CF_4 in O_2 is needed to etch TIPS-PC.

The performance of the organic semiconducting layer is directly influenced by the surface energy and surface roughness of the dielectric layer [19,20]. The interface between TIPS-PC and parylene-C plays an important role in defining the performance of the p-type device. The triisopropylsilyl functionalized groups of the TIPS-PC are hydrophobic, therefore parylene-C was chosen because it creates a hydrophobic surface, with a direct impact on the TIPS-PC microstructure, and therefore the OTFT performance [21]. The solvent also has a direct impact on the TIPS-PC microstructure, and the high boiling point of tetralin (206 °C) has a positive effect on the morphology of the TIPS-PC, maximizing p-type performance [19].

To compensate for the lower TIPS-PC mobility, when compared with that of CdS, the devices (Inverters, NAND gates) are designed with smaller W/L ratios for the CdS TFTs. In order to analyze the individual transistor behavior, isolated transistors were fabricated on the same substrate. Electrical characterization was carried out using a Keithley 4200 semiconductor characterization system. All devices were characterized in the dark under atmospheric conditions. Mobility (μ_{SAT}) and threshold voltage (V_T) were calculated from the slope, and extrapolation of the $I_D^{1/2}$ vs. V_G curve in the saturation regime using the expression below [22]:

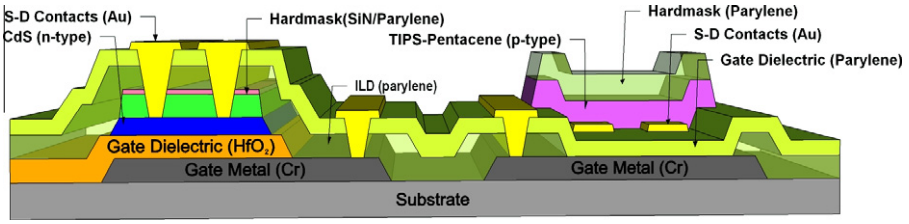

Fig. 1. Cross sectional schematic view of the organic/inorganic hybrid solution-based CMOS device. TIPS-PC and CdS are used as p-type and n-type semiconductors, respectively. Both transistors share gate metal (Cr) and S–D (Au) contacts, reducing the number of photolithography steps to 6 masks.

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