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Organic field-effect transistors with ultrathin modified gate insulator

L.A. Majewski *, M. Grell

Department of Physics and Astronomy, University of Sheffield, Hicks Building, Hounsfield Road, Sheffield S3 7RH, UK

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Abstract

In this communication, we demonstrate high capacitance, low-voltage organic field-effect transistors (OFETs) built on extremely cheap, flexible, commercially available aluminized Mylar® films covered by ultrathin (∼3.5 nm) SiO_2 layers, which were modified via application of *n*-octadecytrichlorosilane (OTS) self-assembled monolayer. The modified SiO_2 was tested as gate insulator in OFETs using pentacene and regioregular poly(3-hexylthiophene) (rr-P3HT) as active materials. The characteristics of the fabricated devices display low threshold (<−1 V) assuring normally "off" transistor operation, very low inverse subthreshold slopes (pentacene: 255 mV/dec, rr-P3HT: 375 mV/dec), good carrier mobility (pentacene: 0.12 $cm^2/(V\,s)$, rr-P3HT: 0.01 $cm^2/(V\,s)$) and a very small hysteresis. The performance of the presented OFETs is high enough for many commercial applications significantly reducing costs of their production.

Keywords: Organic field-effect transistor (OFET); Low voltage; Self-assembled monolayer (SAM); Gate insulator

1. Introduction

A remarkable progress in "carbon based" electronics, especially in the field of organic field-effect transistors (OFETs), has been achieved during the last two years. Excellent examples of OFETs and their integrated logic circuits (ILC) using evaporated and solution processed semiconductors have been demonstrated [1]. However, despite the huge progress in understanding what hinders the performance of OFETs [2], the reported operational voltage of these devices is often too high (30 V or more) causing their integration in cheap, disposable and mobile electronic products rather difficult.

In a FET, the gate voltage, V_G, required to switch the transistor "on" scales with the insulator thickness, *d*, and inversely with the insulator dielectric constant, *k*: $V_G \sim d/k$. Consequently, high *k* at low *d* is desirable. However, both minimising *d*, and maximising *k*, leads to practical problems: a thin, fragile dielectric may lead to increased leakage currents through the insulation layer, and in consequence, rise in power consumption and shorten the device life-time, whereas polar (high-*k*) insulators introduce undesirable effects at the organic semiconductor-insulator interface [3] (disadvantageous morphological changes and increased level of energetic disorder in poly(crystalline) and amorphous materials, respectively) generally leading to increased trapping, which causes a rise of threshold voltage, V_T, and inverse subthreshold slope *S*, as well as, lowers the field-effect mobility of charge carriers in OFETs.

Therefore, the choice of a "proper" insulator is not easy and usually depends on the intended applications. Polymeric OFET insulators (e.g. PVP [4], PVA [5], PMMA [6], BCB [7], etc.) having the advantage to be processed from solution, usually have rather low surface polarities but have to be fairly thick (typically, >100 nm) to avoid formation of pin-holes and their dielectric constants *k* are rather small. This results in insulators with low gate capacitance (order 10 nF/cm^2) and consequently, operational voltages exceeding 30–50 V.

Thermally grown SiO_2 has often been used as OFET insulator, but more for the reason of commercial availability rather than performance, as SiO_2 does not display much higher gate capacitance than polymers ($k \sim 3.9$). Moreover, thermally grown SiO_2 is not flexible and too expensive for

* Corresponding author. Fax: +44 114 272 8079.
E-mail address: php01lam@sheffield.ac.uk (L.A. Majewski).

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disposable electronics. Sputtered metal oxides (Al_2O_3 [8], Gd_2O_3 [9], HfO_2 [10], Ta_2O_5 [11], etc.) usually have higher k than SiO_2 and polymeric insulators, but again, the sputtering process requires expensive vacuum steps which may significantly increase production cost of transistors, and films have to be rather thick to make sure they are free of pinholes. Nevertheless, there are many metallized plastic foils on the market with sputtered/evaporated metals capped, for example, by SiO_2 which retail at <10 €/m^2.

An important concept in the improvement of inorganic oxides for organic transistor applications is silanisation, first introduced into the OFET-field on the example of SiO_2 [12]. Silanes such as *n*-octadecyltrichlorosilane (OTS) can react with –OH groups that are found on the surface of SiO_2 and all metal oxides, to form a self-assembled monolayer (SAM). Silanisation leads to a much less polar interface, and leads to better ordering and partial shielding from the energetic disorder in the case of poly(crystalline) and amorphous materials, respectively, which in result increases carrier mobility, and may dramatically decrease V_T and S in these devices. Additionally, SAMs may smooth rough surfaces, and on very thin insulting layers, reduce undesirable leakage currents [2].

In this contribution, we report on our successful efforts to fabricate low voltage operated OFETs on commercially available, cheap, aluminized Mylar® films that are capped by a thin layer of SiO_2 (∼3.5 nm), which we have modified by the application of an OTS self-assembled monolayer.

2. Experimental

The cross-section of our top-contact devices is shown in Fig. 1. As a substrate, we used commercially available aluminized (Al, ∼60 nm) polyester film (Mylar®, DuPont Teijin Films) covered with a very thin (∼3.5 nm) SiO_2 layer as supplied by Flex Products Inc. (Santa Rosa, CA, USA). The metallized foil is manufactured in the industrial reel-to-reel process, and therefore to achieve a high degree of reproducibility and reliability of the fabricated devices, only the pieces of the film without any visible scratches were carefully chosen. The film was cut into slices (3.5 cm × 1.5 cm), degreased in acetone and methanol (both purchased from Aldrich, UK), carefully washed several times in high purity deionised water

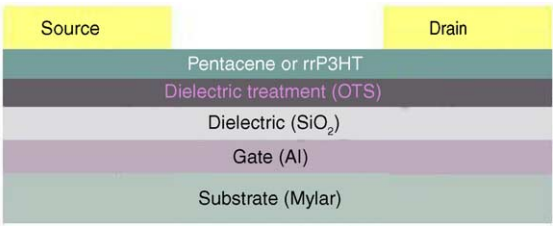

Fig. 1. Schematic structure of the fabricated top-contact OFETs with an ultrathin (∼3.5 nm), OTS-treated SiO_2 layer as the gate insulator (OTS: *n*-octadecyltrichlorosilane).

(Millipore Q, R_s > 1 MΩ cm) and finally dried under compressed air. Subsequently, *n*-octadecyltrichlorosilane (OTS, 90+, Aldrich, UK) was deposited by immersing films in 10^{-3} M of OTS in cyclohexane at 5 °C for 15 min. Directly after OTS treatment, capacitance and breakdown behaviour of resulting structures was measured with the help of evaporated 2 mm × 2 mm, 50 nm thick gold electrodes using commercially available capacitance meter operating at 800 Hz (Iso-Tech 9023). The measurement was repeated on at least four squares. Leakage current and breakdown tests were carried out directly after capacitance measurements using the same connections. The bottom (Al) electrode was biased either positively (as it would be in an n-type transistor) or negatively (as it would be in a p-type transistor). The irreversible breakdown occurred at approximately −2.5 V in both directions (not shown), almost 1 V higher than in the case of unmodified SiO_2 [13]. Pentacene (97%, Aldrich, UK) was used as received without further purification. The material was evaporated under high vacuum conditions (<5×10^{-7} Torr) with nominal rate of 3 Å/s at room temperature (RT). The thickness of the deposited film was controlled during evaporation and also after deposition. Dektak profilometer measurements revealed that pentacene thickness was about ∼45 nm for the samples placed directly above the evaporation crucible. The thickness of the samples placed further was not less than ∼35 nm. Regioregular poly(3-hexylthiophene) (rr-P3HT, Aldrich, UK) was reduced with hydrazine (Aldrich, UK) and spun from 8 g/L solution in chloroform (anhydrous, Aldrich, UK) at 2000 rpm for 60 sec in air. Subsequently, samples were left to dry in high vacuum (<10^{-6} Torr) for 12 h to reverse the well-known effect of oxygen doping. Transistors were completed by evaporation of Au source and drain contacts under high vacuum (<10^{-6} Torr) through a shadow mask on the top of both semiconductors. The channel width/length was 2 mm and 25 μm, respectively. The characterization of the fabricated devices took place in a metal box filled with dry, pure nitrogen. Transistors were contacted via Karl Süss MicroTech PH100 miniature probe heads to two Keithley 2400 source-measure units (SMUs) which controlled source–drain (V_{SD}) and gate (V_G) voltages. The SMUs have a constant current offset of around -2×10^{-10} A which is therefore the smallest current measured reliably.

3. Results and discussion

Capacitance measurements on Mylar®/Al/SiO_2/Au structures revealed relatively high capacitance of ∼1 μF/cm^2 [cf. ref. 13]. After application of OTS, capacitance was reduced to about (305 ± 10) nF/cm^2. The application of SAM ($k \sim 2.5$, $d \sim 2.8$ nm, [14]) inevitably lowers effective capacitance due to formation of an additional capacitor connected in series. Nevertheless, the low operational voltage of transistors ($|V_G| < 2$ V) due to the increased mobility on modified surfaces is still possible.