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Short communication

# Defect annealing processes for polycrystalline silicon thin-film solar cells

S. Steffens[a,*], C. Becker[a], J.-H. Zollondz[b], A. Chowdhury[c], A. Slaoui[c], S. Lindekugel[d], U. Schubert[e], R. Evans[e], B. Rech[a]

[a] Helmholtz-Zentrum Berlin, Berlin, Germany
[b] CSG Solar AG, Thalheim, Germany
[c] L'Institut d'Électronique du Solide et des Systèmes, Strasbourg, France
[d] Fraunhofer-Institut für Solare Energiesysteme, Freiburg, Germany
[e] Suntech R&D Australia Pty Ltd, Sydney, Australia

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ABSTRACT

A variety of defect healing methods was analyzed for optimization of polycrystalline silicon (poly-Si) thin-film solar cells on glass. The films were fabricated by solid phase crystallization of amorphous silicon deposited either by plasma enhanced chemical vapor deposition (PECVD) or by electron-beam evaporation (EBE). Three different rapid thermal processing (RTP) set-ups were compared: A conventional rapid thermal annealing oven, a dual wavelength laser annealing system and a movable two sided halogen lamp oven. The two latter processes utilize focused energy input for reducing the thermal load introduced into the glass substrates and thus lead to less deformation and impurity diffusion. Analysis of the structural and electrical properties of the poly-Si thin films was performed by Suns-$V_{OC}$ measurements and Raman spectroscopy. 1 cm$^2$ cells were prepared for a selection of samples and characterized by $I$–$V$-measurements. The poly-Si material quality could be extremely enhanced, resulting in increase of the open circuit voltages from about 100 mV (EBE) and 170 mV (PECVD) in the untreated case up to 480 mV after processing.



## 1. Introduction

Polycrystalline silicon thin-film technologies are a promising option for cost-effective solar module production, with the potential to exceed the current photovoltaic efficiency limitations of existing silicon based thin-film technologies, and combine the advantages of crystalline silicon (no degradation, high electrical quality) with the advantages of thin film technologies (low cost, low material consumption). Fabrication is done by deposition of less than 2 μm thin silicon layers and a subsequent solid phase crystallization (SPC) process. Necessary prerequisites are excellent electronic properties of these poly-Si films. In order to tap the full potential of poly-Si material, the application of defect healing processes such as rapid thermal processing and hydrogen passivation (HP) is indispensable after deposition and crystallization [1].

Before RTP and HP the material suffers from high defect densities reducing the lifetime of the minority carriers thus limiting the maximum achievable open circuit voltage. This work investigates the influence of three different rapid thermal processing techniques on the performance of polycrystalline silicon thin film solar cells.

Rapid thermal processing has been extensively used over the last two decades for the annealing of point-like and extended defects and activation of dopants in polycrystalline silicon-based solar cells [1–5]. While for these experiments halogen lamp powered ovens and furnaces have been used, new approaches utilize focused energy input to anneal the silicon thin films [6,7]. In this work we explore the potential of new annealing techniques like laser treatment and annealing by focused halogen lamp power compared to a conventional rapid thermal annealing furnace. These methods were applied to polycrystalline silicon thin films deposited by plasma enhanced chemical vapor deposition and electron beam evaporation. Compared to PECVD the latter, being an emerging technology in silicon photovoltaics [8,9], comprises two main advantages, i.e. high deposition rates and the absence of toxic process gases.

All annealing experiments presented in this work have been done in the framework of the European project "PolySiMode" (Improved Polycrystalline-Silicon Modules on Glass Substrates).

## 2. Material and methods

### 2.1. Substrate

SiN-coated borosilicate glass was used as a substrate for the deposition of polycrystalline silicon thin films. 100 nm thick SiN

* Corresponding author. Tel.: +49 30 8062 41385.
*E-mail addresses:* simon.steffens@helmholtz-berlin.de (S. Steffens), hzollondz@masdarpv.com (J.-H. Zollondz).

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layers have been deposited on Schott Borofloat (BF) 33 glass (3.3 mm) by CSG Solar in an industrial PECVD reactor. The SiN serves as anti-reflection coating and diffusion barrier preventing impurities from the glass substrate reaching the silicon films during high-temperature treatments.

### 2.2. Deposition of silicon

On these BF/SiN substrates a stack of silicon layers was deposited, consisting of a highly phosphorous doped 30 nm thick $n^+$ emitter layer, a lightly boron doped 1.6 μm thick $p^-$ absorber layer and a highly boron doped 50 nm thick $p^+$ layer which serves as a back surface field, leading to a sample structure as follows: BF glass/SiN/$n^+$-Si/$p^-$-Si/$p^+$-Si. Deposition of the $n^+$ layer was done by PECVD, the boron doped layers were deposited either by PECVD using a gas mixture of diborane and silane or by electron beam evaporation of silicon material with co-deposition from a boron effusion cell.

Three different combinations of substrate and deposition method were manufactured for this work:

(1) Electron beam evaporation on smooth BF/SiN/n+ substrates
(2) Plasma enhanced CVD on smooth BF/SiN substrates
(3) Plasma enhanced CVD on rough BF/SiN substrates

Roughening of the substrates was done by abrading the deposition side of the Borofloat glass prior to the deposition of the SiN layer. The abrasion etch process involves dry blasting with SiC grit and a subsequent HF etching process as described in [10]. While in PECVD the film's growth is conformal, EBE is a physical vapor deposition method with a directional flux of the silicon atoms. Due to the directionality of the silicon deposition during EBE, rough substrates are non-compatible with this method leading to minor electrical quality [11]. That is why this combination has not been considered here. The silicon layers were deposited in the amorphous phase at a substrate temperature of about 300 °C for both deposition techniques. Finally, the samples were cut into pieces with sizes from of 2.5 cm × 2.5 cm to 5 cm × 5 cm.

### 2.3. Post-deposition treatments

Crystallization of the amorphous layers was done by a solid phase crystallization process at 600 °C with slow heating and cooling rates (1 K/s) under nitrogen atmosphere, leading to grain sizes of up to 5 μm [12,13]. The crystallized samples were then subject to different defect annealing techniques as described below. After annealing all samples were processed in a hydrogen-plasma passivation tool in order to further reduce the amount of electrically active defects [14–16]. An industrial custom-built prototype inline remote plasma system was used where the samples are exposed to atomic hydrogen for 4 min at 610 °C and during 14 min of cooling down to a temperature of 300 °C.

Three different RTP techniques were applied to the above described silicon stacks on smooth and rough glass substrates: A conventional rapid thermal annealing (RTA) oven, a laser annealing (LA) setup and a zone melting recrystallization (ZMR) tool.

#### 2.3.1. Rapid thermal annealing

The RTA system used in this work is the *Heatpulse 210T* from AG Associates. It consists of a quartz chamber, two banks (upper and lower) of tungsten-halogen lamps and a microcontroller unit. The samples are placed on a 4″ graphite carrier, which is situated between the upper and lower row of halogen lamps. There are 13 lamps with a power of 1.5 kW each. Temperatures up to 1050 °C are possible. The maximum and minimum heating rate is 200 K/s and 0.7 K/s, respectively. A thermocouple is installed right next to the sample carrier to monitor the temperature. Its signal is processed by the microcontoller to regulate the temperature profiles. During annealing the chamber is under nitrogen atmosphere.

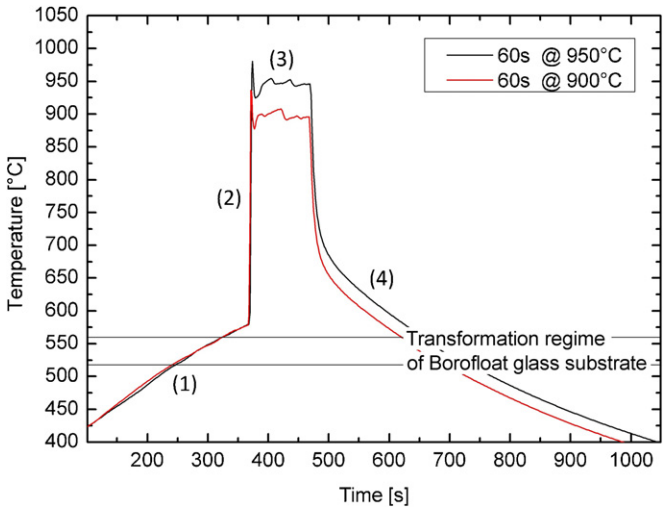


**Fig. 1.** RTA temperature profiles for 900 °C and 950 °C and a plateau time of 60 s. It involves slow heating through the transformation regime (1), fast heating (2) to the plateau temperature (3) and slow cooling through the transformation regime.

For the rapid thermal processing of silicon coated glass samples a temperature profile was chosen that takes into account the transformation range of Borofloat 33. The transformation temperature of Borofloat 33 is 525 °C, the transformation range lies within its strain point (518 °C) and its annealing point (560 °C) [17]. Below the strain point the thermal expansion coefficient of the borosilicate glass of $3.3 \times 10^{-6}$/K matches that of silicon ($2.6 \times 10^{-6}$/K). Within the transformation range the thermal expansion properties of the two materials diverge. The non-linear behavior of the glass' expansion coefficient necessitates slow heating and cooling rates in order to avoid cracking. Above 560 °C the glass softens rendering fast temperature ramps possible.

The samples were treated with temperatures from 900 °C to 1050 °C. The plateau time was varied from 30 s to 150 s. A plot of typical temperature profiles for our annealing experiments at 60 s is depicted in Fig. 1. Note that the plateau time for the thermocouple is 100 s which results in an effective plateau time of 60 s for the 3.3 mm thick Borofloat samples. The thermal mass of the glass substrate also assures that the sample will not follow the overshoots at the beginning of the plateau. The heating phase is divided in two parts: First there is a slow heating ramp (1) through the transformation range. At temperatures well beyond the transformation range, a very fast ramp (2) of more than 150 K/s is applied for heating the system to the desired plateau temperature within a few seconds. This maximum temperature is held constant for the chosen plateau time (3). At the end of the plateau the halogen lamps are shut down to let the system cool down (4) to below 250 °C when the chamber is opened and the samples are removed from the carrier. The cooling rate when passing the transformation range is around ~1 K/s.

#### 2.3.2. Laser annealing

Laser induced annealing was carried out by a dual wavelength set-up (808 nm and 940 nm) manufactured by LASERLINE Inc. with a maximum total power of 3 kW. Prior to the annealing process the samples were preheated to temperatures around 430 °C by a hot plate substrate holder. During laser treatment, the sample holder is moved perpendicular to the line shaped focus. The dimensions of the laser focal line are 0.8 cm × 10 cm. The scan speed of the sample was varied from 40 mm/min to 100 mm/min. Irradiation of the silicon films was done through the glass side with a maximum laser