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High performance low temperature solution-processed zinc oxide thin film transistor

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ABSTRACT

Amorphous zinc oxide thin films have been processed out of an aqueous solution applying a one step synthesis procedure. For this, zinc oxide containing crystalline water ($ZnO \cdot \times H_2O$) is dissolved in aqueous ammonia (NH_3), making use of the higher solubility of $ZnO \cdot \times H_2O$ compared with the commonly used zinc oxide. Characteristically, as-produced layers have a thickness of below 10 nm. The films have been probed in standard thin film transistor devices, using silicon dioxide as dielectric layer. Keeping the maximum process temperature at 125 °C, a device mobility of 0.25 $cm^2V^{-1}s^{-1}$ at an on/off ratio of 10^6 was demonstrated. At an annealing temperature of 300 °C, the performance could be optimized up to a mobility of 0.8 $cm^2V^{-1}s^{-1}$.

1. Introduction

As a potential low-cost alternative for traditional inorganic semiconductor processing, printing of electrical circuits is gaining importance. Printed devices such as radio frequency identification tags or active flat panel displays require high performance thin film transistors (TFTs) preferably processed at low manufacturing temperatures. Stability in air as well as transparency are further specifications which would reduce integration costs and open the market of display electronics. The first TFT based on an organic semiconductor (polythiophene) was demonstrated in the mid 1980s with a field effect mobility (μ_{FE}) of around 10^{-5} $cm^2V^{-1}s^{-1}$ and opened the idea of low temperature processed TFTs [1]. Nowadays, mobilities of organic p-type TFT-devices are in the range of 0.5 $cm^2V^{-1}s^{-1}$, realized using self-organized and aligned layers with partly crystalline domains of conjugated p-type polymers making a 2-dimensional transport possible [2,3]. Even though the mobility of n-type organic devices generally is inferior to p-type devices, an optimization of the interface between dielectric layer and semiconductor lead to n-type polymer transistors with a mobility of 10^{-3} to 10^{-2} $cm^2V^{-1}s^{-1}$ [4] and also exceeding 0.5 $cm^2V^{-1}s^{-1}$ [5].

Nonetheless, the transport properties of functional organic compounds can hardly compete against those of inorganic semiconductors, even if the latter are used in a low crystalline quality. Thus, there are considerable efforts to make inorganic materials printable. For this, function-carrying nanoparticles are stabilized in dispersions and used as inks for printing processes. After depositing the ink on a substrate, the solvent evaporates and the particles remain loosely packed in a thin film. First n-type all-inorganic printable thin film transistors used cadmium selenide (CdSe) nanoparticles as semiconductor [6] and reached a mobility of 1 $cm^2V^{-1}s^{-1}$. Devices with active layers made of lead selenide (PbSe) [7] and mercury telluride (HgTe) [8] nanoparticles were realized. Albeit successful proof-of-principle, the introduction of such devices into a mass market is not unproblematic because of environmental concerns.

Against this background, zinc oxide (ZnO) is attracting attention as an environmentally friendly, conditionally air stable and transparent semiconductor for both, high-end electronic applications as well as the low cost sector. Field effect mobilities of sputtered ZnO thin films are commonly around 20–30 $cm^2V^{-1}s^{-1}$ [9,10], but values up to 70 $cm^2V^{-1}s^{-1}$ have also been reported [11]. Single nanowire transistors of ZnO show mobilities between 30 $cm^2V^{-1}s^{-1}$ [12] and up to 96 $cm^2V^{-1}s^{-1}$ [13]. The combination of single ZnO nanowires with organic electronics demonstrated basic operation of a hybrid solar cell [14].

For low cost electronics, attempts have been made to develop solution-based deposition techniques and the corresponding precursor chemistry for ZnO thin films in order to demonstrate the feasibility of printing processes. Solution processed thin film transistor devices [15–19] or ultraviolet photodetectors [20] have been demonstrated. Their performance still is competitive with amorphous silicon.

Volkman et al. [15] used dispersions of ZnO nanoparticles. Dense ZnO layers were obtained by spin coating and annealing, yielding device mobilities of 0.2 $cm^2V^{-1}s^{-1}$. Sun and Sirringhaus [16] similarly produced ZnO-nanoparticles and nanorods in stable dispersions. After layer formation and additional hydrothermal ZnO-growth,

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devices showed a mobility around 0.6 $cm^2V^{-1}s^{-1}$. There are also several approaches for solution-based process with liquid precursors, without the intermediate step of nanoparticle formation. Bashir et al. [19] solved a zinc acetate dihydrate precursor directly in methanol. Layer formation by spray pyrolysis was combined with varying substrate temperatures up to 600 °C. Device performance was optimized to best values of the mobility of $\mu = 15\ cm^2V^{-1}s^{-1}$. Li and co-workers [17] used an aqueous solution of zinc nitrate, hexamethylenetetramine, and water. For layer formation, they heated the sample within the solution. Using a bottom gate device structure with a high-k dielectric layer, a device mobility of 0.56 $cm^2V^{-1}s^{-1}$ was shown. Meyers and co-workers [18] also used zinc nitrate as precursor. It was solved in a strong base, NaOH, to form the hydroxide $Zn(OH)_2$. The supernatant was removed by centrifugation and the precipitate re-suspended in H_2O. This procedure was repeated several times to reduce the concentration of ions. The obtained product was dissolved in ammonia, NH_3(aq). Layer formation was done by spin coating, followed by an annealing step. Mobilities between 0.4 and 6 $cm^2V^{-1}s^{-1}$ were shown, depending on annealing temperature and the type of the dielectric layer.

Common of the cited work is that the preparation of the zinc precursor solution usually requires several steps of purification or substrate temperatures which are too high to be compatible with flexible substrates. Here we show that the time-consuming purification procedure can be overcome by the use of a zinc oxide hydrate ($ZnO \cdot \times H_2O$) precursor which has a sufficient solubility in ammonia due to the crystal water. This leads most probably to a similar ammine-hydroxo zinc complex $Zn(OH)_x(NH_3)_y^{(2-x)+}$ in aqueous solution, as described by Meyers and co-workers [18], however in a simple one step procedure. This precursor solution can be transformed to amorphous ZnO-thin films at a temperature of 125 °C, well suitable for the purpose of printable electronics. Taking benefit of these properties, a simple one-step fabrication procedure for high performance low temperature solution-processed zinc oxide thin film transistors is demonstrated.

2. Experimental details

The commercially available zinc oxide hydrate, $ZnO \cdot \times H_2O$, of (Sigma-Aldrich, 97% purity), shows a sufficient solubility in NH_3 which has its origin in the crystal-water. For the herein used thin films, the ZnO precursor solution was varied between 0.04 and 0.07 molar solution of $ZnO \cdot \times H_2O$ in NH_3(aq) (Sigma-Aldrich, ≥99.99% purity, 28% in H_2O). For most devices a 0.05 molar solution was used. The solution was kept at 40 °C under rigorous stirring for 48 h. This yielded a clear transparent liquid which was filtered using a 700 nm glass filter. The thin-film formation was carried out by spin coating at 3000 rpm followed by an annealing step for 60 min in ambient atmosphere to convert the ZnO precursor. The annealing temperature was varied between 125 °C and 500 °C, with 125 °C being the standard annealing temperature. In order to improve the layer morphology and device performance the film forming step has been partially doubled (indicated in the text). For the device fabrication, phosphorus doped silicon wafers ($3 \cdot 10^{17}\ cm^{-3}$) with thermally grown SiO_2 of 200 nm thickness were used. Substrates were cleaned and made hydrophilic before spin coating. After the layer formation, source and drain aluminum electrodes were deposited by physical vapor deposition through a shadow mask. Electrode spacing was 100 μm and width 7.4 mm. The electrical characterization was carried out under the exclusion from ambient light in a nitrogen filled glovebox using a Keithley parameter analyzer 4200-SCS in combination with a probe station. In order to study the layer morphology, electron transparent lamellae of two transistor-samples were prepared using focused ion beam (FIB, FEI Helios Nanolab). A platinum layer was deposited on top of the devices using ion beam induced decomposition prior to the FIB sample preparation to protect the device from the ion beam. The lamellae were investigated with an FEI Tecnai F20 equipped with an energy dispersive X-ray (EDX) system and a GIF2000 energy filter. Optical transmission was measured in an UV–VIS spectrometer Lambda 9 from Perkin-Elmer.

3. Results and discussion

ZnO thin films were processed by spin-coating a 0.05 molar precursor solution of zinc oxide hydrate, $ZnO \cdot \times H_2O$, in NH_3 as described above onto Si/SiO_2 substrates. Subsequently, the thin films were annealed at 125 °C under ambient conditions. Some of the devices were processed in a way, that the procedure of spin-coating and annealing was repeated. This double spin-coating procedure includes: spin-coating a precursor solution onto a Si/SiO_2 substrate, annealing at 125 °C, spin coating the same precursor solution a second time onto the already processed ZnO layer, and annealing at 125 °C.

The film morphology was exemplarily investigated by transmission electron microscopy (TEM) on a FIB lamella prepared from a ZnO transistor produced by double spin coating and annealing at 125 °C. Fig. 1a shows a TEM image of the stack. The active layer (ZnO) together with the gate oxide (SiO_2) and one of the electrodes (Al) can be distinguished. The ZnO layer is uniformly smooth over the whole lamella—several micrometers of the device could be investigated by TEM with no defects found whatsoever. The thickness of the ZnO thin film is around 7 nm, the thickness of the evaporated Al-contacts around 54 nm. Fig. 1b shows an energy filtered bright-field image of the same sample. Part c shows an EDX line scan over the stacked layers. The very sharp Zn-signal can again be assigned to a layer thinner than 10 nm. An additional X-ray diffraction investigation was carried out (not shown), where an amorphous film was found.

Fig. 1d shows the cross section of a transistor sample after single spin-coating and annealing at 500 °C. A ZnO crystallite of a size larger than 20 nm is shown, the presence of ZnO crystallites was observed along the whole lamella.

The transistor characteristics of two different devices are shown in Fig. 2. In Fig. 2a and b, the ZnO thin film was processed by a single spin coating step of the 0.05 molar precursor solution as described above and subsequent annealing at 125 °C. For the transistor characteristics shown in Fig. 2c and d, the active layer was obtained by doubling the procedure (spin coating, annealing at 125 °C, spin coating, annealing at 125 °C). A clear enhancement mode for positive gate bias and linear progression in the saturation regime combined with a moderate hysteresis is demonstrated for both devices. By doubling the spin coating and annealing, a higher drain current, less hysteresis, and a clear reduction in threshold voltage is yielded compared to the singly spin coated sample.

The mobility μ_{FE} was derived from the transfer characteristics in Fig. 2b and d, respectively. In the linear regime with the drain current I_{lin}, the curves were fitted to the Eq. (1):

$$\frac{\partial I_{lin}}{\partial V_G} = \mu_{FE}\ g(V_D - x). \tag{1}$$

The factor g contains the gate dielectric capacitance and the electrodes geometry, x denotes the x-axis shift, while V_G and V_D are the applied gate and drain voltages. For the saturation regime (subscript *sat*) at higher source-drain bias, the square root plot of the drain current was fitted to the Eq. (2) with the drain current I_{sat} and the threshold voltage V_{th}:

$$\frac{\partial \sqrt{I_{sat}}}{\partial V_G} = \sqrt{\mu_{sat}\ g}(V_G - V_{th}). \tag{2}$$

Table 1 summarizes the obtained data for the two devices shown in Fig. 2. It can be seen that by doubling the layer formation step, μ_{FE} can be increased significantly from $\mu_{FE} = 0.12\ cm^2V^{-1}s^{-1}$ (single