



Substrate- and oxidation-induced roughness of individual terraces of pentacene thin films

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ARTICLE INFO

Article history:

Received 8 July 2010

Received in revised form 30 September 2010

Accepted 7 October 2010

Available online 21 October 2010

Keywords:

Surface roughness

Organic semiconductor

Degradation

Scanning force microscopy

ABSTRACT

The roughness at the surface of *individual pentacene terraces* on naturally oxidized silicon wafers was investigated with scanning force microscopy as function of film thickness (one to five layers) and sample exposure to ambient air. For pristine samples, the root-mean-square roughness on individual (001) pentacene terraces was 0.18 nm and varied by less than 0.02 nm between monolayer terraces and terraces in the fifth layer. Storing samples in air and ambient light led to a substantial increase of the roughness, which for terraces up to the third layer became 0.24 nm after four weeks. For fourth layer terraces, the roughness increased less, and terraces in the fifth layer exhibited no significant roughness increase. We explain the roughness increase by photo-oxidation of pentacene, particularly strong within the first layer, which is supported by the appearance of grain boundary widening with storage time. The observation that layers beyond the third one from the substrate are less affected by photo-oxidation (smaller terrace roughness) is likely due to better structural perfection in layers farther from the substrate, which reduces the effective cross-section of molecules for oxidation. These results indicate that native silicon oxide does not allow for the immediate formation of structurally perfect pentacene films in the range of one to three layers, which will reduce charge carrier mobility in pentacene thin film transistors. Thicker pentacene layers can protect underlying layers against oxidation.

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1. Introduction

Pentacene thin films are of general interest for applications in organic electronics because they serve as *the* model system for investigations of organic thin film growth and charge carrier transport, most notably in a thin film field-effect transistor geometry. Pentacene thin films have shown exceptional high crystallinity and concomitantly high charge carrier mobility of up to $6.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is in the range of the values for amorphous silicon, and therefore of great technological relevance [1–3].

The electrical properties of a thin-film organic field-effect transistor (OFET) are largely determined by the current which flows in close vicinity to the semiconductor/gate-insulator interface [4–8]. Several research groups have studied the thickness dependence of the charge carrier mobility in thin pentacene films [6,8]. The common result is that the mobility saturates at a thickness of only a few pentacene layers, i.e., nominally six layers in the cases of Ruiz et al. [8] and Kiguchi et al. [6]. Consequently, the morphology and crystallinity of such interface-near layers determine the charge transport behavior in OFETs.

Upon deposition of small molecules onto a substrate, e.g., by thermal evaporation, film formation is governed by nucleation and growth. Therefore, the resulting morphology depends strongly on a variety of chemical and physical parameters, such as substrate temperature, deposition rate, or the kinetic energy of the molecular beam [9,10]. It has been pointed out that the roughness of the gate dielectric as a substrate has an impact on the field-effect mobility of pentacene OFETs [11–15], and also on conjugated polymers [16–20] or nanoparticle [21] transistors. Generally, it has been found that the field-effect mobility – in some cases beyond a certain roughness threshold – decreases with increasing dielectric roughness. This has been explained in terms of charge carriers being accumulated in nano- and mesoscopic “valleys” of the gate dielectric due to the transverse gate field, leading to a “positional trapping” within these valleys [13,14,20,21]. An alternative picture for crystalline organic materials is that the surface diffusion of the molecules is impeded by roughness, leading to higher nucleation density, reduced grain size and therefore a higher density of grain boundaries that the charges have to overcome in the OFET channel [13,16,19]. Moreover, Kang et al. [22] have modeled the roughness of pentacene layers in terms of a molecular displacement along the long axis in a pentacene crystal (maintaining the 2D herringbone packing in the substrate plane), and they have shown that such vertical packing imperfections induce shallow trap states for both electrons and holes. This implies that substrate-induced roughness of molecular layers can severely alter

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the electrical properties of OFETs in terms of mobility and on-set voltage.

Another important aspect is the exposure of conjugated organic films to ambient conditions, which has shown to be detrimental to their electrical properties in terms of unwanted doping and material decomposition [23–27]. The exact nature of the degradation in the presence of oxygen and in conjunction with moisture and/or visible or UV light is still not fully understood. However, a number of studies indicate that the responsible mechanisms involve reversible (at short time-scales, typically a few hours) and irreversible (at longer exposure) processes [24,27–30], both of which are attributed to the interaction with reactive oxygen species (O_2 , O_3 , or even O_4). For pentacene films, it was reported that besides electrical degradation, long-time exposure to aggressive oxidants, such as ozone, leads to a significant mass-loss of the pentacene film due to the formation of volatile reaction products [27,29].

Here we present a study on the *roughness evolution on individual terraces*, in contrast to the roughness of the entire film, including the layer heights, as a function of pentacene film thickness up to five layers on naturally oxidized silicon wafer surfaces. The roughness of the substrate is reflected in the roughness of the pentacene terraces. We further investigated the effect of long-time ambient exposure on the roughness of these terraces, and we infer that photo-oxidation is affecting films up to three to four pentacene layers, while the fifth layer is already significantly less affected. Furthermore, photo-oxidation takes place preferentially directly at grain boundaries, where oxygen has an easier access to the most reactive reaction sites of a pentacene molecule.

2. Experimental details

High-grade pentacene was used as received (Sigma-Aldrich), and thermally evaporated in high vacuum ($p < 10^{-4}$ Pa) onto silicon substrates (from Siegert Consulting eK, prime grade, p-doped), covered with native oxide, at a rate of 0.1–0.2 nm/min as controlled by a quartz-crystal microbalance.

Surface topography was investigated using a Digital Instruments NanoScope IV atomic force microscope (AFM) operated in Tapping-Mode™. For accurate roughness determination, sufficiently high resolution was assured by recording 512 points/line at a slow scan rate of 1 line/s. Cantilevers (Olympus) had a typical spring constant of 42 N/m. The measurement of pristine pentacene layers was performed immediately after deposition. To further minimize the effects of (photo-)oxidation on these layers, the sample and AFM setup were covered by a light protection hood during measurement. Roughness analysis was done with the software package SPIP (ImageMetrology).

The root-mean-square (rms) roughness (simply termed roughness in the following) was determined by

$$r = \sqrt{\frac{1}{N} \sum_{k=1}^N (z_k - \bar{z})^2},$$

where z_k is the height information at each of the N data points, and $\bar{z}$ is the mean image height.

To study the influence of ambient exposure at application-relevant conditions, the respective samples were stored in laboratory air (shielded from dust) being subjected to indirect sunlight exposure during daytime.

3. Results and discussion

Fig. 1 shows AFM images of pentacene on native silicon oxide samples with different nominal film thickness. Overall in our study, we investigate films that nominally comprise 0.5, 1.5, 2.5, 3.5, 4.5 and 5.5 layers of nearly upright standing molecules. It is typical for the film growth of pentacene on weakly interacting surfaces to take place in an almost layer-by-layer fashion for the first two layers [8,9,31,32]. Subsequently, island-growth sets in, leading to the formation of terraced incomplete pentacene layers, as can be seen in Fig. 1c. The cross-section height profiles show that the step-height of the pentacene terraces is constantly (1.48 ± 0.02) nm for all film thicknesses. On native silicon oxide, pentacene usually grows in the “thin-film phase” with a (001) texture, which is characterized by a nearly upright orientation of the long molecular axis with respect to the substrate plane [9,11,27,32–38]. The “bulk phase” often forms at larger thicknesses exceeding some tens of nanometers, where the actual critical film thickness depends on the substrate temperature [9,11,36]. Both polymorphs have in common that pentacene is arranged in a herringbone fashion within a layer of almost standing molecules. The crystal lattice parameters of the thin-film phase have been a matter of debate in the literature, however, reports consistently give $d_{001} \approx 1.55$ nm for the inter-plane spacing of the pentacene layers [9,27,32–36]. This is in close agreement with our value for the terrace height; the difference with respect to the X-ray investigations is due to the systematic error (calibration error) of the AFM measurements. The visual appearance of the pentacene layers strongly indicates that the terrace surfaces have a certain roughness that is evident at all film thicknesses for all stacked layers. In earlier publications such apparent roughness of pentacene terraces was sometimes evident, in some other publications not because of specifically applied image coloring schemes. A zoom into the image of the 0.5 layer sample shows (Fig. 1a) that the oxidized silicon surface

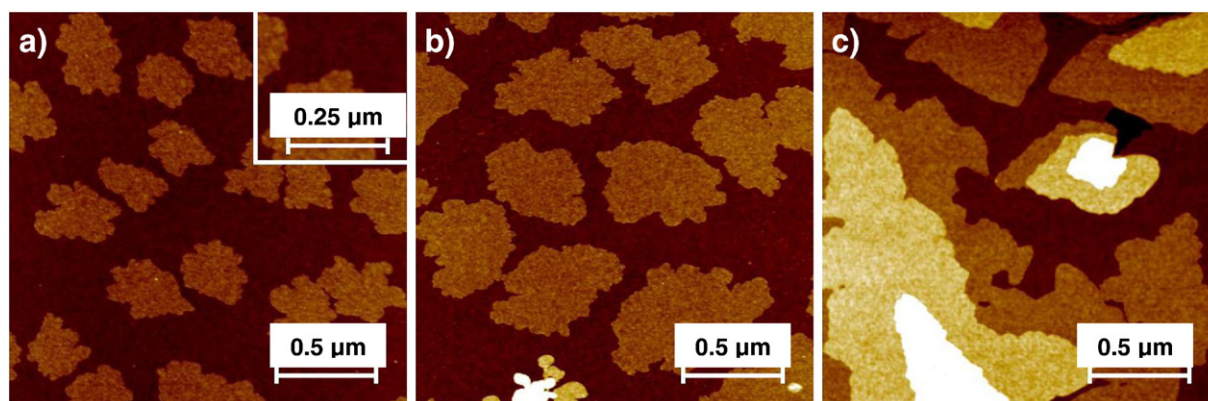


Fig. 1. $2 \mu\text{m} \times 2 \mu\text{m}$ AFM topography images of fresh (non-degraded) pentacene films on naturally oxidized silicon with nominal thicknesses of a) 0.5 pentacene monolayer (ML), b) 1.5 ML, and c) 5.5 ML. The inset of a) is a magnification to stress the pentacene roughness.

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