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A scanning microscopy technique based on capacitive coupling with a field-effect transistor integrated with the tip

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ABSTRACT

We propose a method for measuring the capacitance of a thin layer using a Tip-on-Gate of Field-Effect Transistor (ToGoFET) probe. A ToGoFET probe with a metal–oxide–semiconductor field-effect transistor (MOSFET) with an ion-implant channel was embedded at the end of a cantilever and a Pt tip was fabricated using micro-machining. The ToGoFET probe was used to detect an alternating electric field at the dielectric surface. A dielectric buried metal sample was prepared; a sinusoidal input signal was applied to the buried metal lines; and the ToGoFET probe detected the electric field at the tip via the dielectric. The AC signal detected by the ToGoFET probe was demodulated by a simple AC-to-DC converter. Experimentally, it was shown that an electric field could be measured at the surface of the dielectric layer above a buried metal line. This promising result shows that it is possible to measure the surface local capacitance.

1. Introduction

The electrical properties of surfaces are of great interest for researchers in a broad range of science and engineering fields. In particular, the semiconductor industry has used a number of measurement techniques to evaluate the physical characteristics of semiconductor devices. Frequently used characterization techniques include scanning electron microscopy (SEM) [1], transmission electron microscopy (TEM) [2], and secondary ion mass spectroscopy (SIMS) [3]. More recently, various scanning probe microscopy (SPM) techniques have become widely used in semiconductor device characterization [4], including electrostatic force microscopy (EFM) and scanning capacitance microscopy (SCM).

Both EFM and SCM rely on a micro-cantilever with a conductive tip. The electrical properties of dielectric films, including the dielectric constant, film thickness, and electronic properties of trap states, can be measured using SCM [5], and the electric potential distribution at the surface can be measured using EFM. SCM measures the spatial variation in the capacitance, whereas EFM measures the electrostatic reaction force between the probe tip and the surface [6]. We have previously introduced SPM techniques to characterize the electric potential and bound charge distribution at a surface using the custom-built ToGoFET Probe [7]. With that method, the electric potential or the charge distribution may affect the conducting tip, which is in electrical contact with the gate of a field-effect transistor (FET), so that the source–drain current depends on the surface electric potential or charge density. Here, we extend that technique by applying an alternating voltage to the surface and the probe tip so that the gate voltage is affected by the capacitance of the surface locally. This may be considered as an SCM mode of microscopy using the ToGoFET probe because it uses an applied AC voltage (as SCM does), in contrast to previously reported techniques [10].

Many custom probes that employ FETs have been proposed for measuring the electrical properties of surfaces [7–9]. Among them, Lee et al. proposed a method employing an FET on a flat surface of a cantilever, with a sharp tip mounted on the gate of the FET [7]. We term this arrangement a tip-on-gate-of-FET (ToGoFET) probe because of the structure. The ToGoFET probe has a number of important advantages for characterizing the electrical properties of surfaces that result from the geometry of the system and the measurement mechanism. Because the FET is located on the probe and the metal probe tip is in electrical contact with the gate of the FET, the surface electric potential could be characterized with high spatial resolution. It follows that the local electrical properties can be detected and amplified with greater sensitivity than with other surface measurement systems, including electrostatic force microscopy (EFM), Kelvin probe force microscopy (KPFM), and SCM. With the ToGoFET probe, the signal is less affected by environmental electrical noise, which leads to a high signal to noise ratio (SNR). Because the surface electric properties are measured using an FET-based probe, the ToGoFET probe can be used to detect the

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electrical properties of the surface without electrical losses, and complicated and expensive electrical circuits are not required. Furthermore, this measurement system can be used to detect time-varying electrical properties. These advantages have led us to adapt and improve the capabilities of the ToGoFET probe.

Here, we report a method to measure the capacitance of a dielectric layer using the ToGoFET probe. A metal line was prepared, on top of which a dielectric passivation layer was deposited. An AC bias was applied to the buried metal line and, upon scanning the surface, the AC signal was measured using the ToGoFET probe. The AC signal induces a charge at the tip, which in turn leads to a variation in the potential of the channel of the ToGoFET probe. Consequently, the source–drain current flowing through the channel of the FET is modulated by the AC signal. The gate of the ToGoFET probe is floating electrically, and current due to the AC signal flows only between the sample and the tip, in contrast to an SCM system, in which the current flows in a resonance circuit through the cantilever. Because of the large impedance of the gate of the FET, the amplitude of the current is much smaller. The ToGoFET probe can detect very small variations in the charge, however, because of the inherent sensitivity of the FET.

We fabricated a ToGoFET probe embedded with an ion-implanted metal–oxide–semiconductor FET (MOSFET), where the threshold voltage was designed for efficient transduction of the electrical signal at the probe tip. The resulting ToGoFET probe was evaluated with a sample formed from a diamond-like carbon (DLC) dielectric layer deposited on the metal lines. The thickness of dielectric layers used in SCM measurements is typically in the range several nanometers to several tens of nanometers [11], and the corresponding capacitance of the dielectric layer per unit area is of the order of several mF/m^2. We measured the surface of a dielectric layer that was 200-nm thick, and where the capacitance per unit area was only 170 $\mu F/m^2$ theoretically, which is approximately one tenth of that reported using SCM. For a 200-nm-thick dielectric, the induced charge at the tip should be approximately one tenth of that which can be measured using SCM. For a sample with a capacitance per unit area of 170 $\mu F/m^2$, the scanning ToGoFET probe showed particularly promising results for characterizing spatial variations in the capacitance.

2. The ToGoFET probe

2.1. Principles of operation

The ToGoFET probe consists of a V-shaped cantilever, a MOSFET, and a conductive nano-scale tip, as shown in Fig. 1. The ToGoFET has four contacts: the gate (G), drain (D), source (S), and reference (B). The structure of the probe is such that the tip is mounted on the gate of the FET, and when the tip makes contact with the surface of the sample, a current can flow to the gate contact via the nano-tip. The surface potential induces a charge at the tip due to the local electric field, which determines the source–drain current. As a result, we can directly infer the electrical properties at the surface using the ToGoFET probe.

When the ToGoFET probe is used to scan a dielectric with buried metal lines with an applied AC signal, as shown in Fig. 1(a), there is an electric field between the conducting metal tip and the buried metal layer. With an AC signal, separation and redistribution of the charge will occur in such a way that the surface of the metal tip is maintained at a constant potential. Away from the tip, the electric-field lines will intersect the surface normally; the electric field is concentrated at the tip because of the sharp profile, whereas there is no electric field inside the tip. The charge at the tip, Q_T, is distributed at the end due to the concentrated electric field. At the surface of the gate electrode, a charge Q_G (with opposite sign to Q_T) is induced in such a way that the electric field inside the tip vanishes. The induced charge Q_G at the gate electrode of the ToGoFET probe results in an electric field across the gate oxide layer, which modulates the channel of the FET. In this way, variations in the charge at the tip result in a change in the source–drain current in the FET.

The capacitance, C, describes the amount of charge Q held at a potential V. It is defined as the electric charge that must be added per unit increase in the electric potential, and is given by the ratio $C=Q/V$. The capacitance is a function of the geometry of the conducting materials and the permittivity of the dielectric separating them. When the ToGoFET probe makes contact with the surface of the dielectric, the amount of charge that is induced at the tip is related to the AC bias at the buried metal line, as well as the capacitance between the buried metal line and the tip. This capacitance may be modeled by considering a spherical metal tip and the permittivity of the dielectric layer [10]. When the

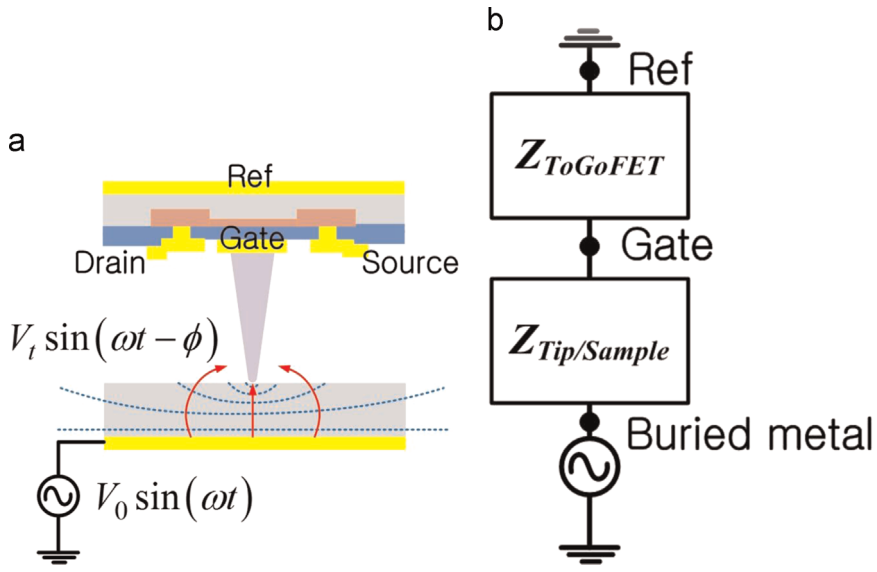

Fig. 1. A schematic diagram of measurement system and its impedance model. (a) A schematic diagram showing the measurement system using the ToGoFET probe. (b) The impedance model used to infer the capacitance.