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Changes in surface layer of silicon wafers from diamond scratching

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ABSTRACT

This study investigates diamond scratching at a high speed comparable to that in a grinding process on an ultraprecision grinder. Diamond tips are prepared for the study. The scratched silicon wafer is observed for changes in the surface layer with transmission electron microscopy. The observation discovers that an amorphous layer is formed on top of the pristine Si-I phase before the onset of chip formation. This discovery is different from the previous findings in which a damaged silicon layer is identified underneath the amorphous layer. Furthermore, no high pressure phase is found before the onset of chip formation.

1. Introduction

Single diamond grit scratching is a fundamental approach to investigating surface integrity in wire sawing, grinding, lapping, polishing, and nanogrinding [1–3]. In an abrasive machining process, a machined surface is obtained after multiple passes of abrasives, which leads to the difficulty in achieving deterministic surface integrity achievable in a single-point machining process. At present, three techniques are employed to simulate the single grit scratching: the first is diamond scratching with a developed micro-actuator device [1]; the second is machining with the atomic force microscopy (AFM) [2]; and the third is scratching with a commercial nanoindenter [3]. These techniques have promoted our understanding on surface integrity associated with the ultraprecision machining processes, both scientifically and technologically. The scratching speeds used in the three techniques were 1 mm/min [1], 5 μm/s [2], and 3.3 μm/s [3], respectively, which is five to six orders of magnitude lower than that used in a typical abrasive machining process, such as wire sawing (5–20 m/s) [4], and grinding (14.1–40.3 m/s) [5,6]. Furthermore, high speed scratching at a nanometer depth of cut is another challenge.

In addition, how to identify the onset of chip formation from a scratching process, and the changes in the surface layer are extremely difficult. High speed scratching at the m/s speed level and the nanometer depth of cut using a single diamond tip has not yet been explored. Nevertheless, Ruffell et al. [7] have demonstrated that scratching speeds play an important role to surface integrity of the brittle materials. Consequently, it is necessary to perform high speed scratching at the nanometer depth of cut to investigate surface integrity involved in the nanofabrication of silicon wafers.

Silicon (Si) is abundant, non-toxic, and has an appropriate bandgap of 1.1 eV [8], dominating the solar cell and microelectronics industries [9]. Photovoltaic solar cells based on the crystalline silicon account for more than 85% of the market share today [10]. Manufacturing process has a significant influence on the cost for a solar cell. For instance, wire sawing wafers from a silicon ingot is up to 15% of the overall cost of a solar cell [11]. Moreover, ultraprecision grinding in the fabrication of silicon wafers is critical to the whole cost of a solar cell [5,6].

This study explores the surface integrity of a silicon wafer subjected to a high speed scratching experiment at the nanometer depth of cut. The scratching experiment is carried out on an ultraprecision grinder. Three diamond tips are fabricated with a tip radius in the submicron range for the study.

2. Experimental details

Natural diamonds produced in South Africa with weight ranging from 0.1 to 0.2 carats were used as the diamond tip materials. According to the natural texture of the diamonds, the hardest orientation was identified and marked. A similar hole based on the size of the diamond grit was machined in the head of a carbon steel lever to hold the diamond grit. Nickel-based alloy was filled in the gap between the diamond and the lever. A graphite rod drilled in a hole to the size similar to the diamond grit was used to press the marked face during a high-frequency welding process. In preparing the diamond tips, grinding was conducted on the precision grinder. Diamond tips were prepared with resin bond diamond wheels of grit sizes of 40, 20, 5 μm, then a vitrified diamond wheel of grit size of 2 μm, and finally, a low carbon steel plate for finishing. With this approach, three pyramidal diamond tips with a submicron tip radius were developed. To obtain a

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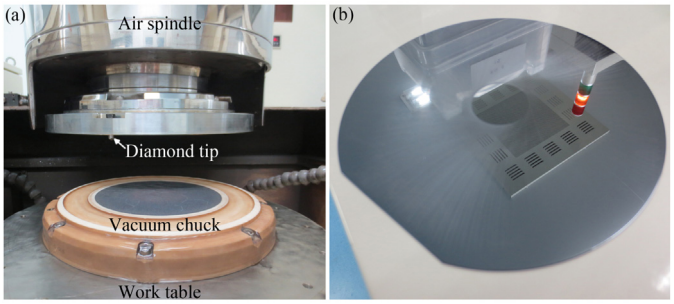

Fig. 1. Optical images of (a) a diamond tip fixed onto the ultraprecision grinder and (b) a scratched silicon wafer.

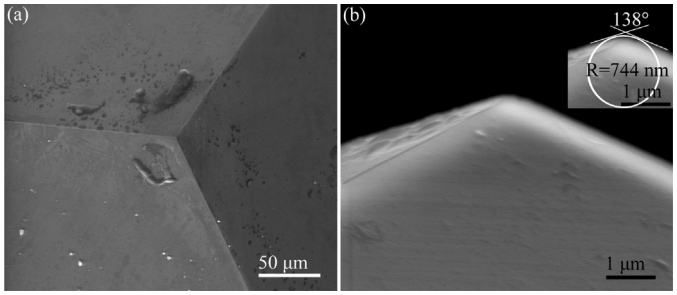

Fig. 2. Top (a) and side (b) views of diamond tip A after scratching silicon wafers at 15 m/s. Inset in (b) shows the included angle and filet radius.

nanometer tip radius, a ground diamond tip was further polished by focused ion beam (FIB) (FEI, Nova 200 Nanolab) at an accelerated voltage of 30 kV. Polishing current was set first to 7 nA and then to 100 pA.

The developed diamond tip was fixed on an aluminum alloy plate of a diameter of 320 mm, and mounted on an ultraprecision grinder (Okamoto VG401 MKII, Japan), as shown in Fig. 1(a). Commercial silicon (1 1 1) wafers with a diameter of 150 mm were used as specimens. A silicon wafer was fixed on the ultraprecision grinder by a vacuum chuck. High speed scratching at a nanometer depth of cut was performed using a variation of 150 nm between face runout of 50 nm of the air spindle and flatness of 100 nm of the commercial silicon wafer. The initial contact between the diamond tip and the silicon wafer was identified manually through the subtle scratching tracks on the silicon wafer. The digital readout of the air spindle at the contact position was taken, and then the air spindle was uplifted for 15 μm, rotated and fed downward at a feed rate of 1 μm/min. The high speed scratching conditions are shown in Table 1. When the downward feeding reached the setup value, the wheel was uplifted instantaneously, and the scratching process was ended. During scratching, no coolant was applied in order to obtain scratched chips (debris) on the silicon wafer surface. A sample of the scratched Si wafer is shown in Fig. 1(b).

Three diamond tips were characterized by scanning electron microscopy (SEM) (Lyra3 Tescan, Czech Republic) equipped with FIB prior to and after the high speed scratching on the silicon wafers. Listed in Table 1 are the included angle and tip radius of the diamond grits after the high speed scratching. The three-faceted pyramidal (3FP) diamond tips were designated as diamond tips A and B at a scratching speed of 15 and 8.4 m/s, respectively. The four-faceted pyramidal (4FP) diamond tip polished by FIB is assigned as diamond tip C. Scratch width at the onset of chip formation and width and depth at the onset of crack formation on a silicon wafer were measured by SEM (Lyra3 Tescan), followed by an in situ FIB etching. Transmission electron microscopy (TEM, FEI Tecnai F20) samples were prepared using FIB (FEI, Helios600i). TEM examinations were conducted at an accelerated voltage of 200 kV.

3. Results

Fig. 2 shows the top and side views of diamond tip A after scratching silicon wafer at 15 m/s. It is observed in Fig. 2(a) that three facets meet at one point, indicating the sharpness of diamond tip A. Its included angle was 138°, similar to a Berkovich tip (142.35°), and tip radius is 744 nm.

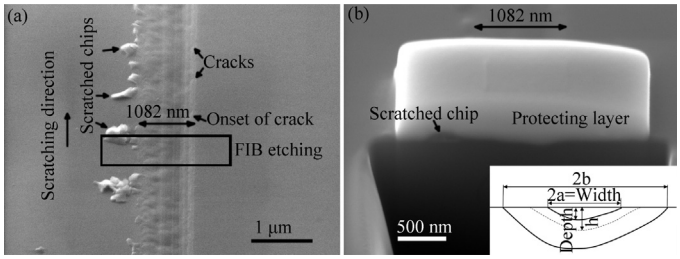

Fig. 3. Onset of crack formation induced by diamond tip A (a) and (b) in situ FIB etching of the area marked with a black window in (a). Inset in (b) shows the schematic of width, depth, inelastic size and deformation of the scratch.

Fig. 3 depicts the scratch at the onset of crack formation and its corresponding SEM images from the FIB etching. The scratch width and depth at the onset of crack formation were 1082 nm (Fig. 3(a)) and 61 nm (Fig. 3(b)), respectively. The scratching chips were discontinuous. The onset of crack formation was followed by two other cracks, shown in Fig. 3(a). FIB etching was in situ carried out perpendicular to the silicon surface to measure the scratched depth and prepare TEM samples at the onset of crack formation.

A layer of amorphous phase silicon was identified on top of the pristine diamond cubic Si-I phase, as shown in Fig. 4(a) and (b). The Si-I phase was further confirmed with the selected area electron diffraction (SAED) in Fig. 4(a). Fig. 4(c) shows the amorphous phase at the topmost, followed by a damaged layer beneath. SAED in Fig. 4(c) verifies the Si-I phase in the damaged layer (Fig. 4(d)). Edge dislocations were found in the damaged layer, but no nanocrystals were observed in the amorphous phase (Fig. 4(a) and (c)).

Fig. 5 shows SEM images of diamond tip C in top and side views. Diamond tip C polished by FIB had an included angle of 117°, and tip radius of 92 nm. Fig. 6 presents SEM images at the onset of crack formation induced by diamond tip C and the same sample after the in situ FIB etching. The width and depth of the scratch at the onset of crack formation were 1104 and 120 nm, respectively. The onset of crack formation was followed by another crack (Fig. 6(a)). Discontinuous chips were observed, shown in the inset in Fig. 6(a) adjacent to the onset of crack formation.

In Fig. 7(a) and (b), amorphous phase is found at the topmost, and pristine diamond cubic Si-I phase is underneath. At the location of the onset of crack formation, the amorphous phase was in the top layer, followed by a damaged layer underneath (Fig. 7(c)

Table 1
High speed scratching conditions.

Diamond tip (shape)	Included angle (°)	Radius of curvature (nm)	Width at the onset of chip formation (nm)	At the onset of crack formation		Wheel speed (m/s)	Table speed (rpm)	Feed rate (μm/min)
				Width (nm)	Depth (nm)			
A (3FP)	138	744	321.1 ± 13.8	1096.2 ± 28.4	56.3 ± 7.9	15	80	1
B (3FP)	140	344	262.5 ± 12.6	1124.7 ± 31.2	54.1 ± 7.4	8.4	80	1
C (4FP)	117	92	164.9 ± 10.5	1108.4 ± 21.6	122.3 ± 15.6	8.4	80	1