

Early works on the nuclear microprobe for microelectronics irradiation tests at the CEICI (Sevilla, Spain)

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ABSTRACT

Particle radiation effects are a fundamental problem in the use of numerous electronic devices for space applications, which is aggravated with the technology shrinking towards smaller and smaller scales. The suitability of low-energy accelerators for irradiation testing is being considered nowadays. Moreover, the possibility to use a nuclear microprobe, with a lateral resolution of a few microns, allows us to evaluate the behavior under ion irradiation of specific elements in an electronic device. The CEICI is the new Center for Integrated Circuits Irradiation tests, created into the facilities at the Centro Nacional de Aceleradores (CNA) in Sevilla-Spain. We have verified that our 3 MV Tandem accelerator, typically used for ion beam characterization of materials, is also a valuable tool to perform irradiation experiments in the low LET (Linear Energy Transfer) region.

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1. Introduction

Small electrostatic heavy-ion accelerators (under 5 MV) are very common facilities in Universities around Europe. Most of them also have microprobe endstations because they are extremely useful for material and biological studies. The microprobe community [1,2] realizes the relevance of nuclear microscopy also for reliability studies of microelectronics under heavy ion irradiation. As it is well known from the SEE (Single Event Effect) ESA/SCC 25100 standard [3], a SEE test is comprised of a heavy ion accelerator, the chip under test and the test system. This paper presents the early works at the Accelerator National Center, CNA, in Spain, in order to adapt its microprobe facility for SEE studies. We also report a SEU (Single Event Upset) LET threshold experiment on a digital test chip, using a new test system, FT-Rad [4].

There are several test systems for SEE testing of RAM memories based on FPGA (Field Programmable Gate Arrays), for example STREAM [5,6]. SEE RAM memory testing is a static test because there is full observability of the memory state. In a general digital circuit the access to the circuit state has to be inferred from the outputs in real time, therefore necessarily the test has to be dynamic. FT-Rad is able to make SEE dynamic tests of general digital circuits.

At CNA we use a 3 MV tandem pelletron to generate oxygen microbeams from 14 to 18 MeV. The test chip was designed specifically as test vehicle, using the low-priced 0.6 μm integration scale,

very well known in the SEE community [7,8]. The test chip has three cores, modelling the typical subsystem hierarchy presented in integrated circuits, hence the use of a microprobe is justified in order to limit radiation only to specific built-in-chip subsystems. The focusing ability of the microprobe, for example, could be very useful to irradiate the digital subsystem of a mixed-signal chip without irradiation of the analog blocks.

In section 2 we explain the ion radiation experiment arrangement. Section 3 is dedicated to present the FT-Rad tool suite and the specificities associated to radiation testing of digital ASIC's (Application Specific Integrated Circuits). Final section 4 presents the experiment results and the performance of the FT-Rad tool suite.

2. SEU experiment setup

The CNA facility has a 3 MV tandem accelerator, model 9SDH-2 from NEC, the ion source is a SNICS II, also from NEC and the microprobe is an Oxford MicroBeam endstation OM2000, equipped with the usual instrumentation for IBA (Ion Beam Analysis) techniques in material research, see Fig. 1 [9]. Low-LET accelerators have been used before for SEU testing, [10].

The beam is directed to a microchamber where we use mainly three instruments, see Fig. 1: a 20x optical microscope, a PIPS detector ($\theta = 0^\circ$) and a Si(Li) detector for PIXE ($\theta = 135^\circ$). The light from a ZnS(Ag) scintillator foil is observed by means of the optical microscope. The PIXE detector registers the X-Rays induced by ion impact on the chip silicon and on a 25 μm copper microgrid. The

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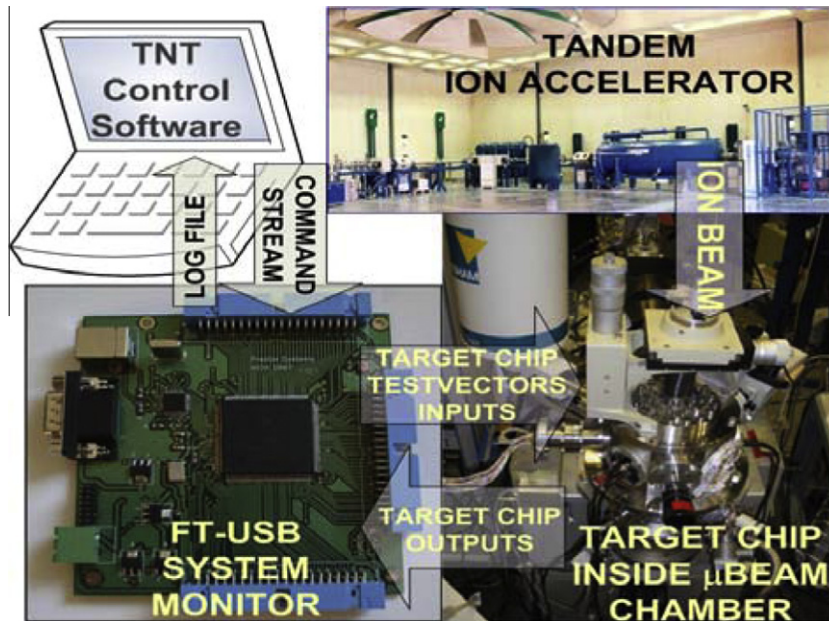


Fig. 1. Experiment layout. Ions from the tandem impinge on the target chip inside the microbeam chamber. FT-USB generates run signals for the target chip and registers all the chip outputs. A laptop is used as human machine interface.

scintillator foil and the microgrid are adhered to the chip by means of an aluminium pedestal.

For beam stability purposes, we monitor the beam state with a Beam Profile Monitor during the test. Using the PIPS detector we measure the ion current before the target chip is in position. With the ion beam activated, the particle counter output feeds a charge amplifier to generate a signal for the Single Channel Analyzer. The SCA outputs counting pulses, processed by a rate meter.

With the experiment running, the particle counter is behind the target chip so it cannot be used. During the experiment, the constancy of the X-ray event count was also monitored as an indirect mean to know about the ion current stability. The X-rays event count rate of the PIXE detector was calibrated in a nonfunctional part of the chip, looking at the 1.7 keV Si line. We select the Si line because there is plenty of silicon in the target chip and because it gives a strong X-ray emission under ion irradiation of the chip.

The scintillator optical signal shows the beam spot shape at the target plane. In order to estimate the spot area we observe the X ray image of the beam spot at the Cu microgrid. With the spot calibrated, the target area is selected using the optical microscope and positioned in the spot by means of a micrometric XYZ screw.

Considering also the tandem accelerator and the ion source instrumentation it is possible to select specific ion species, with a fixed charge state, kinetic energy, flux and to collimate the spot in the target area. The spot can also be in scan mode, with a scan frequency of 10 KHz but in our experiment we did not use the scan mode, only a fixed spot on target.

A dedicated 3.3 V digital ASIC has been designed and built for this experiment, using a 0.6 μm (gate length) CMOS AMSC5 process from Austria Mikro Systems. AMSC5 is a CMOS commercial-like technology, available through the MOSIS programme [11], fabricated on epitaxial substrates with local oxidation of silicon (LOCOS) for field oxide isolations. CMOS technologies on 0.6 μm scale are well known in the radiation test community [8], with a threshold LET for SEE around 7 MeV cm^2/mg . For example, in [7] it is shown the threshold LET ($\approx 7 \text{ MeV cm}^2/\text{mg}$) and also the full upset cross-section (see for example [12] for a discussion of the upset cross-section concept) for a 256K SRAM built with the CMOS6 process, a VLSI technology also with 0.6 μm integration scale.

Our selected integration scale for the test chip takes advantage of that previous knowledge.

As test vehicle, a functional model has been conceived which allows to identify from its output patterns which flip-flop undergoes a bitflip due to an ion impact. The chip has three identical cores with that functional model, see Fig. 2. That design has enough complexity to generate dynamics and its output patterns are simple enough for calibration of FT-Rad. It is comprised of a shift register (SR), a pair of XOR matrices and four parallel to serial converters (PS). The XOR matrices generate a parity bit from the SR content, so a bitflip in the SR is detected by the XOR and given as extra input to the PS registers.

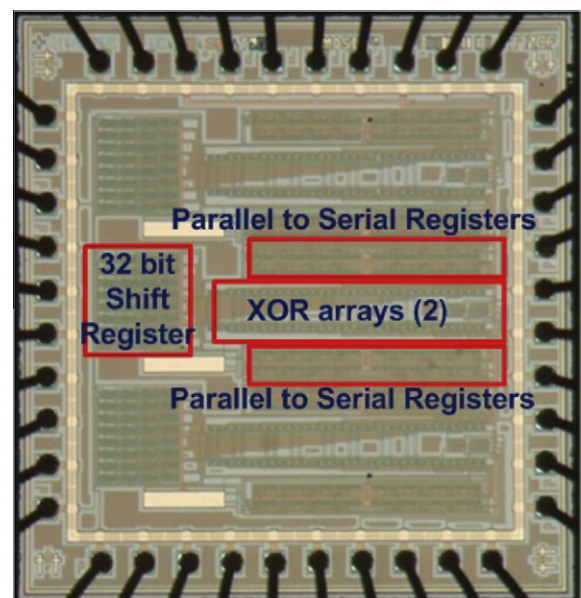


Fig. 2. The target chip is an Application Specific Integrated Circuit, ASIC, designed in 0.6 μm integration scale. It comprises three identical cores, central core highlighted. See Fig. 3 for core details.

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