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Advanced monolithic quantum well infrared photodetector focal plane array integrated with silicon readout integrated circuit

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Abstract

Today, most infrared focal plane arrays (FPAs) utilize a hybrid scheme. To achieve higher device reliability and lower cost, monolithic FPAs with Si based readout integrated circuits (ROICs) are the trend of the future development. In this paper, two approaches for monolithic FPAs are proposed: double sided integration and selective epitaxy integration. For comparison, the fabrication process for hybrid quantum well infrared photodetectors (QWIP) FPAs are also described. Many problems, such as the growth of QWIPs on Si substrate and processing incompatibility between Si and III–V semiconductors, need to be solved before monolithic FPAs can be realized. Experimental work on GaInAs/InP QWIP-on-Si is given in this paper. A record high detectivity of 2.3×10^9 cm $Hz^{1/2}$/W was obtained for one QWIP-on-Si detector at 77 K.

Keywords: Monolithic; Focal plane array; Quantum well infrared photodetector; GaInAs; InP; Si substrate

1. Introduction

Quantum well infrared photodetectors (QWIPs) have become a competitive technology for infrared detection since infrared absorption due to intersubband transition was first observed in multiple quantum well (MQW) structures [1,2]. The detection wavelength of QWIPs can be tuned easily from mid-wavelength infrared (MWIR) to very-long-wavelength infrared (VLWIR) by engineering the MQW structure. Infrared cameras based on QWIPs have been successfully designed and fabricated in the past ten years [3,4]. Those cameras

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have found many applications ranging from military night vision to medical imaging [5]. Due to its ability to operate at very high frequencies [6], QWIPs can be also utilized in some high-speed optical communication applications. Currently, most QWIPs are fabricated on GaAs (e.g. AlGaAs/GaAs) or InP (e.g. GaInAs/InP) substrates, which are the obvious choices for III–V-based QWIPs. To achieve thermal imaging, QWIP detector arrays are hybridized with silicon based readout out integrated circuits (ROIC) so that the detector signal can be read out to external processing circuitry. A number of FPA hybridization techniques exist, such as direct hybrid, indirect hybrid, and loophole [7]. Direct hybrid is the most widely used hybridization technique in infrared FPA fabrication. In direct hybrid, each detector pixel is bonded to a readout circuit unit cell directly via an indium bump in a process called flip chip bonding. With the increase in the size and pixel density for infrared FPAs, the interconnection reliability for hybrid FPAs becomes a major problem. This is mainly due to the large thermal mismatch between Si and GaAs or InP substrates and the difficulty achieving highly uniform indium bumps across the whole array region.

Many advantages will arise if the QWIP could be directly grown on a Si substrate, such as higher thermal conductivity and mechanical strength, the availability of large-area substrates, and thus, lower cost infrared FPAs. Growth of QWIP on Si substrate is the key for the monolithic infrared FPAs with Si ROICs. In this paper, two unique approaches for monolithic QWIP FPA integration with Si ROIC are described. For comparison, the hybrid QWIP FPA fabrication process is described first. Experimental work on GaInAs/InP QWIPs grown on silicon substrate is given following the discussion of monolithic FPA fabrication.

2. Direct hybrid infrared FPA fabrication process

Before the monolithic FPA with Si is given, it is necessary to have a complete knowledge of the commonly used direct hybrid FPA fabrication method. In this section, the normal direct hybrid infrared QWIP FPA fabrication process will be described step by step [8,9]. A schematic of the whole fabrication process is given in Fig. 1. Only one detector pixel is shown in Fig. 1.

1. *QWIP structure growth*. Infrared FPA fabrication starts with the QWIP structure growth, which can be performed by metalorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) technology. The material quality of QWIP structure basically determines the final FPA's performance.
2. *Fabrication of detector pixels*. This includes UV-photolithography for the sample patterning and etching (e.g. ECR-RIE dry etching or wet chemical etching) for the pattern transfer. For large format FPAs, the pitch size is usually between 25 and 40 μm. The detector pixel size is even smaller. A higher fill factor (ratio of pixel area to unit area) is always pursued for this step. However, the fill factor is basically determined by the photomask and ROIC design requirements.
3. *Detector pixel passivation*. SiO_2 or Si_3N_4 are common passivation materials. Selection between SiO_2 and Si_3N_4 is determined by the spectral response of QWIP device [10]. The deposition of SiO_2 and Si_3N_4 can be performed by plasma enhanced chemical vapor deposition (PECVD).
4. Patterning and etching of the passivation layer. The purpose of this step is to make openings for the metal connection to each detector pixel. The opening size depends on the pixel size. The common bottom contact is generally made at the edge of the whole array. To achieve higher indium bump uniformity, the bottom contact is usually realized by short-cutting the top contact layer with the bottom contact layer at the bottom contact mesa (such as with a large square ring around the whole array). Using this scheme, all the indium bumps can be made at the same altitude.
5. Top and bottom contact metallization. Metallization can be done by either lift-off or etch back techniques. For QWIPs, the same ohmic contact metal is usually used for both the top and bottom contact so that only one metallization process is required.