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A new real-time processing system for the IRFPA imaging signal based on DSP&FPGA

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Abstract

The principle, configuration and special features of a new high-precision real-time signal processing system for Infrared Focal Plane Arrays is presented in this note. A structure based on DSP&FPGA is adopted in the system. The FPGA implements the system timing control and the low level algorithms. The DSP performs the high-level algorithms, such as nonuniformity correction for the IRFPA. Nonuniformity correction and image enhancement and display algorithm, the two crucial algorithms for IR imaging signal processing, are also discussed in this note. The experiments on real IR imaging sequences demonstrate that the system is suitable for the real-time high-speed IR imaging system with high quality and high precision.

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Keywords: Infrared Focal Plan Arrays; Infrared imaging; Nonuniformity correction; Image processing; DSP; FPGA

1. Introduction

With the development of Infrared focal plane array (IRFPA) technology, the advantages of high density, excellent performance, high reliability and miniaturization are available in Infrared (IR) imaging systems [1]. At present, acquisition of high quality images has become the key problem of IR imaging systems. Such systems generally need to process mass data in real-time [2]. The processing includes various algorithms, such as nonuniformity correction, image segmentation, local characteristics extraction, image de-noising, image enhancement, etc. hence then must be one well integrated high-speed information processing system. In this paper a new IRFPA imaging system based on the DSP&FPGA is presented to fulfill such requirements.

Our note also focuses on two algorithms that are used in the IR image processing stage. One is the nonuniformity correction and the other is image enhancement and display method. Nonuniformity correction is a key problem that must be first solved in IRFPA systems. The detector-to-detector responsivity (gain) and dark current (offset)

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variations [3–7], which cause the nonuniformity, may completely mask the useful thermal signatures in an IR image with a fixed pattern "noise". In order to get better resolution, a 12 or 14 bit ADC is commonly adopted in the signal processing system [2]. How to effectively map 12 or 14 bit data to 8 bit TV video data is another important technology in IR image processing systems [8,9].

2. New real-time processing system for IRFPA imaging signal

2.1. Hardware configuration of the system

The schematic diagram of the real-time signal processing system for IRFPA imaging based on DSP&FPGA is shown in Fig. 1. The main function unit of the system consists of an IRFPA driving circuit, an analog imaging signal processor, an ADC, a high-speed signal processor, a DAC and a video synthesizer, etc.

The IRFPA driving circuit unit provides the pulse-driving signal and the offset voltage, which are crucial for the IRFPA operating state. It makes the IRFPA work at the optimum operating point. In the traditional method, the driving circuit would be complex and nonflexible. In our system, the driving-pulse signal is achieved by an FPGA. The method has the advantages of high reliability and flexibility.

The pre-processing circuit unit amplifies the imaging analog signal with low noise to the level that the ADC requires. The ADC transforms the analog image signal to a digital one. In order to be applied to image data processing with high speed and precision, a 12 bit ADC whose sampling frequency is up to 20 MHz is selected, so that a high resolution of digitized image data is obtained.

The synchronization and timing control unit harmonizes the other units in the system, including the output circuit unit of the IRFPA, the ADC sample unit, the data store, the DSP, the DAC, the video synthesizer, etc.

The DSP&FPGA unit is the kernel of the system. In the system of real-time IR signal processing, the low-level processing algorithms that only need simple computation deal with a large amount of data. But they do not need high-processing speed. The FPGA is adapted to doing these, and flexibility is also achieved. The high-level algorithms process smaller amounts of data, but are more complex. The DSP (ADSP21060) has the characteristics of high-speed operation, flexible addressing method and powerful communication capability. Thus the DSP is perfect for implementing the high-level algorithm. The memory must be expanded for storing a large amount of IRFPA imaging data. In this note, SRAM is used as expanded data memory, which has the advantages of fast access and lager capacity in a single chip. As an embedded DSP system, the off-chip program memory is also needed. FLASH memory is the preferred choice, which can do online erasing and programming. It also enhances the flexibility of the system.

The image data processed by the DSP&FPGA module are sent to the DAC through a data buffer, where the digital image data are transformed back to an analog image signal. Under the Synchroni-

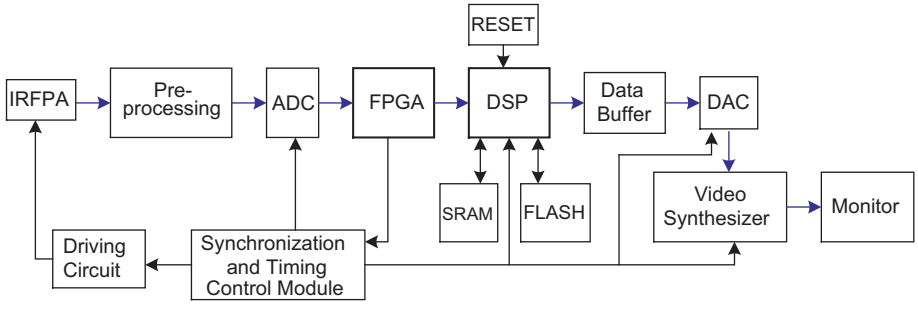

Fig. 1. Schematic diagram of the signal processing system for IRFPA imaging.