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A full on-chip, low noise, low power consumption reference generator in monolithic active pixel sensors

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ABSTRACT

The monolithic active pixel sensor (MAPS) is a promising choice to track charged particles in high energy physics experiments, such as the solenoidal tracker at RHIC (STAR). In order to achieve a clean reference voltage and simplify the cable placement, a full on-chip reference generator is presented in this paper. By utilizing a buffer and a series RC network, the proposed circuit can achieve good stability, low power and low noise, without any external components. The output voltage is adjustable to compensate the influence of the fabrication process. The generator has been implemented and fabricated in a standard 0.35 μm CMOS process. Its silicon area is 327 μm × 119 μm. The total power dissipation is 677 μW at a supply voltage of 3.3 V. The measured results show that only 5.84% of the total noise in MAPS is induced by the proposed reference generator. The comparison with the other optional circuit based on a current buffer is also presented.

1. Introduction

Vertex detectors are proposed to be equipped with the monolithic active pixel sensors (MAPS) in some high energy physics experiments, e.g., the STAR upgrade at RHIC (relativistic heavy ion collider). The MAPS offer an attractive trade-off among many performance parameters, such as, readout speed, granularity, material budget, power dissipation, radiation tolerance and integrating readout circuitry on the same substrate, compared with the charge coupled devices (CCDs) and the hybrid pixel sensors [1–3]. Another important advantage is that MAPS can be thinned to less than 50 μm, which is greatly helpful to satisfy the extremely low material budget. In order to achieve a vertex pointing resolution of about 30 μm or better in the heavy flavor tracker (HFT) upgrade, for the STAR experiment at RHIC, the two internal layers (PXL, also called PIXEL) in Fig. 1 will be equipped with a module composed by 400 MAPS chips called ULTIMATE. Each ladder will be equipped with ten closely mounted MAPS chips (2 cm × 2 cm) [2,4,5]. All the external voltages required have to be supplied from the discrete electronics at the end of the ladders. Thus, the distance between the discrete electronics and the MAPS in the other end is at least 18 cm. It is very difficult to achieve a precise and low-noise reference voltage in this case. To address this problem, some critical reference voltages are proposed to be generated on-chip. The clamping voltage is the most critical reference voltage in the pixel level. Actually, in the pixel the influence of the clamping voltage noise is not suppressed by the correlated double sampling (CDS), the main noise-suppression technique in MAPS [6]. Consequently, it is essential to design a full on-chip, low noise and low power consumption reference generator for the clamping voltage.

The linear regulator is generally utilized as a reference generator. It should feature low-noise and low-power performances. However, stability is the most critical issue in linear regulator designs, especially for relatively large load capacitances. The capacitive and resistive loads of the clamping voltage will be discussed in detail in next section.

Several works about the frequency compensation of linear regulators have been presented in Refs. [7–9]. The traditional "pole splitting" scheme using the Miller capacitor is mostly used [7]. However, the Miller effect is weakened when the load capacitance increases. The compensation capacitor must be very large to achieve a good stability. A compensation scheme based on a current buffer has been discussed in Ref. [8]. Nevertheless, the current buffer consumes high power as well as introduces noise, which is amplified by the output stage. Pole-zero cancellation techniques are widely used in the commercial linear regulators. The zero is usually introduced by an external output capacitor and its equivalent series resistance (ESR). However, the ESR varies with factors such as temperature, DC bias and operating frequency. In addition, this scheme needs an external capacitor. To solve this problem, Silva-Martinez et al. utilized a

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voltage-controlled current source (VCCS) after the output to generate an internal zero [9]. The noise performance has been improved but the power dissipation is still high due to the VCCS, which is realized as a current mirror. All of these methods cannot completely meet the requirements of MAPS.

Our work focuses on the design of a full on-chip linear regulator for this application. It must be stable with different sizes of pixel array for reusing. In addition, low noise and low power consumption are also required. This paper is organized as follows. Design considerations at system level are presented in Section 2. Section 3 describes the circuit design according to the requirements in Section 2. Simulation and measurement results are given in Section 4. Section 5 finally concludes this work.

2. Design considerations at system level

In their most recent versions, MAPS are composed of pixel array, row selector, column-level discriminators, zero suppression, regulators and so forth. The simplified pixel topology is shown in Fig. 2 [2]. The charge sensing elements in pixels collect the charges induced by the ionizing particles. These charges are converted to voltage signal of about a few millivolts by the diode capacitance [1]. The gain of the following preamplifier is only 5–10, which is limited by the pixel size. Consequently, the signal is very sensitive to the noise. To efficiently suppress the pixel-to-pixel and column-to-column fixed-pattern-noise (FPN), the CDS operation is implemented at the pixel level and at the column level [6]. The value of the capacitor C_1 is chosen large enough (about 100 fF, which is about 10 times more than the collecting electrode capacitance) to decrease the KT/C noise during clamping operation. However, the clamping voltage noise is directly injected into the readout node during the reset (CLAMP) phase. Thus, the CDS operation cannot eliminate the influence of this noise and the clamping voltage must be sufficiently clean to prevent signal corruption due to the noise. Furthermore, the clamping voltage must be constant to guarantee the correct CDS operation.

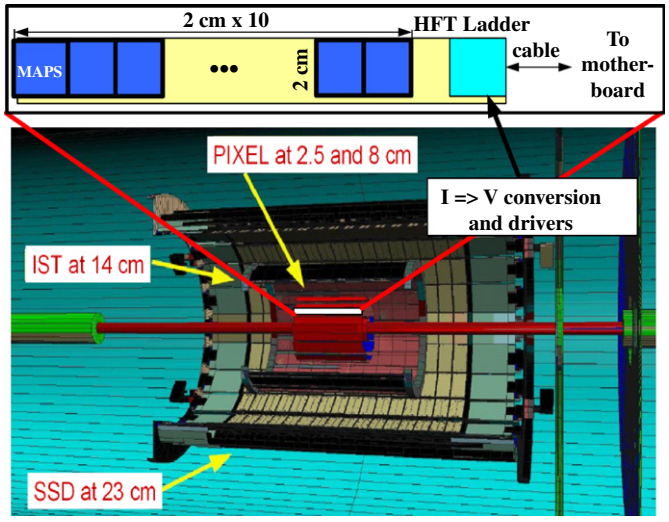

Fig. 1. Heavy Flavor Tracker (HFT) and the diagram of one ladder.

Since the clamping voltage is connected to every pixel in MAPS, its load capacitance drastically increases with the pixel array size due to the parasite. The parasitic capacitance is composed of the internal capacitance in pixel and the wire capacitance, which is the main parasitic source. According to the parasitic extraction from layout, the total capacitance is about 0.5 nF in a 136×576 pixel array. It increases to about 5 nF when the pixel array is 928×960. The on-chip regulator to be designed should fulfill the stability requirements in presence of such a large load capacitance.

Compared with the large capacitive load of clamping voltage, its resistive load is almost zero. The DC load current is not required because there is no DC path to ground, as shown in Fig. 2. Since the pixels are readout in rolling shutter mode, a dynamic current of a few hundred microamperes is sufficient to charge the internal capacitor in one row. In addition, the clamping voltage is usually at least a threshold voltage (about 0.6 V) less than the power-supply voltage (*Vdda*) so that the following source follower can work in saturated region and the switch transistor M1 can work in linear (triode) region to behave like an ideal switch. It is possible to employ a relatively small output transistor due to the small current and output voltage.

Finally, the regulator is required to be compact and low-power due to the small die area of non-sensing elements and the air cooling system, respectively. Since the clamping voltage is very critical to the CDS, its value must be adjustable to compensate the influence of process parameter fluctuations.

The block diagram of the proposed circuit is illustrated in Fig. 3. The regulator is composed of three stages: the error amplifier, the level shift buffer and the output stage. A source follower (SF) operated as level-shift buffer, and a series RC network are inserted to improve the phase margin. The buffer also enhances the transient response. Since the output voltage is directly determined by the feedback resistor, resistor R_A is adjustable to compensate the output voltage values for process fluctuations. The register RV $< 3{:}0 >$ can be accessed by the joint test action group (JTAG) standard interface. The stability analysis will be given in the following subsections. The noise analysis and power supply rejection ratio will also be discussed.

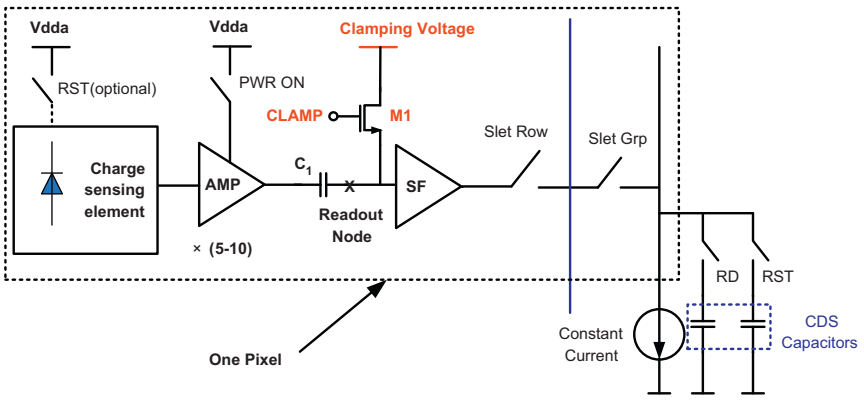

Fig. 2. Simplified pixel topology of MAPS.