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Effect of interconnect geometry on the evolution of stresses in a solar photovoltaic laminate during and after lamination

W.J.R. Song, S.K. Tippabhotla, A.A.O. Tay, A.S. Budiman*

Xtreme Photovoltaics Laboratory (XPV Lab), Singapore University of Technology and Design, Singapore 487372, Singapore

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ABSTRACT

Fracture in silicon crystalline solar cells has been a long-standing challenge encountered in the photovoltaic (PV) industry. This occurs as result of stresses developing in the cells due to thermo-mechanical stresses that arise when there is a mismatch in the coefficient of thermal expansion (CTE) between the different constituent materials during the manufacturing processes as well as mechanical stresses from hail, snow and wind during field operations. Through finite element simulations, this paper investigates the effect of interconnect cross-sectional geometry on stresses developed in silicon cells during the entire PV manufacturing cycle and provides physical reasoning to its stress evolution. The simulations are performed in a sequential manner whereby the residual stresses developed at the end of one step is brought forward to the beginning of the next step. It is found that the highest cell stresses occur at the back surfaces of the cells at the end of the pressure-ramping step during lamination. In addition, increasing the thickness of the front interconnects significantly increases the stresses developed in the cells during lamination. This predicted trend is verified experimentally.

1. Introduction

As the silicon photovoltaic (PV) industry matures, there is a continuous effort to reduce the production cost by increasing the efficiency and reliability of PV modules. During the 1990s, these modules needed a lifetime of about 15–20 years to achieve grid parity when compared to other conventional energy resources [1]. Recently, with highly automated production lines and increasing module sizes, manufacturers have shifted their focus towards reducing the levelized cost of electricity by means of module design. Some of these new designs include back-contact cells, multi-busbar cell interconnection and thinner cells [2–5]. These new designs have an effect on the cracking of silicon cells which are brittle in nature and intrinsically populated with microcracks. These cracks can further propagate when residual tensile stresses act on the cleavage planes during the manufacturing, installation and field operation of PV modules. This is undesirable as such cracks cause unconnected cell areas which result in significant power losses over time [6–8]. In this paper, we will focus on the evolution of stresses in the fabrication of conventional multi-busbar (multi-interconnect) wafer-based silicon solar PV module, and the effect of interconnect geometry on cell stresses.

1.1. Evolution of stresses in solar PV modules

As the cracking of solar cells is due to stress, the study of thermo-mechanical stresses induced in solar cells during the manufacturing processes as well as during field operations has been extensively performed by researchers, both experimentally and computationally. The process of soldering the interconnect to the cell induces stress in the silicon cells. Due to the high temperatures required to melt solder, the differences in coefficient of thermal expansion (CTE) between the cell, interconnect and solder result in high residual stresses when it is cooled to room temperature. A study by Kraemer et al. [9] investigated the effect of such stresses in silicon cells after the soldering of interconnects. Further, Budiman et al. [5] used synchrotron X-ray microdiffraction to elucidate the stress concentration due to the solder in the back-contact design of a SunPower monocrystalline solar cell in the encapsulated state. This group has since pioneered the systematic study of stress evolution and thus, crack propensity using the combination of the synchrotron technique as well as finite element (FE) simulations [10–14].

There have also been many numerical studies which calculate the post-lamination residual thermal stresses in PV laminates. These studies usually assumed a stress-free state of the laminate at the lamination temperature. For instance, Dietrich et al. [15] carried out finite element

* Corresponding author.
E-mail address: suriadi@alumni.stanford.edu (A.S. Budiman).

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(FE) simulations to investigate the thermomechanical stresses of encapsulated silicon cells after lamination, due to differences in CTE of the constituent materials.

Lee and Tay [16] performed 3D FE simulations of a full-scale 72-cell PV laminate to obtain the residual thermal stress distribution in the laminate after the post-lamination cooldown process. The stress redistributions within the laminate subjected to installation and exposure to 1000 W/m^2 of direct sunshine were also simulated. They found that the largest peeling stresses occurred at the edges of the cell-EVA interfaces, a possible location for the initiation of delamination [17].

The residual stress in a PV laminate is actually the result of the accumulation of residual stresses from each segment of the manufacturing cycle. Although the post-soldering stresses and the post-lamination stresses have been calculated in the earlier studies, they have been calculated separately and not been integrated. To properly obtain the accumulated stresses in a PV laminate, each step of the laminate manufacturing cycle should be simulated in a sequential manner whereby the residual stresses developed at the end of one step is brought forward to the beginning of the next step. Tippabhotla et al. [10] performed numerical simulations where the post-soldering stresses were appropriately integrated with the subsequent lamination stresses and post-lamination cooldown stresses, in a sequential manner. They found that high stresses arose due to localised bending of the cells during the lamination process. They verified their findings by comparing with values of stress in the cells measured using synchrotron X-ray submicron diffraction. However, they have only considered a single-cell module with a cell design based on a back-contact monocrystalline silicon cell from SunPower which is a non-conventional interconnect design and not so prevalent.

1.2. Effect of interconnect geometry on module performance and reliability

It has been established that interconnect (busbar) geometry can affect the electrical performance of PV modules. The optimisation of cell performance and busbar configuration was proposed as early as 1978 by Serreze [18]. In his study, Serreze demonstrated that the optimal width of a busbar can be achieved when the resistive loss is equal to the shadowing loss. This led to the finding that a width-tapered busbar design (Fig. 1) is more optimal than a regular rectangular busbar as it has lower resistive losses.

It has also been established that decreasing the width of interconnects can reduce the footprint of the interconnects and hence reduce shadowing losses. However, in order to maintain the electrical resistance of the interconnects, the cross-sectional area of the interconnect has to be maintained, resulting in an increase in the thickness of the interconnect. This may result in higher stresses in the cells during and after lamination. Schneider et al. [19] have carried out experiments which investigated the effect of interconnect thickness, encapsulant thickness and lamination pressure on cell reliability. Mini-modules were subjected to thermocycling and the respective EL images as well as fill factor (FF) losses were recorded. The findings from the study indicated that a thicker interconnect and a thinner encapsulant had an adverse effect on cell cracking and finger to busbar interruptions, resulting in significant power losses.

Thus, this paper has been written in order to clarify the effect of interconnect geometry, in particular its cross-sectional width and thickness, on the evolution of cell stresses during and after lamination of a conventional silicon wafer-based PV laminate. The evolution of such stresses is simulated in a sequential manner whereby the residual stresses developed at the end of one step is brought forward to the beginning of the next step, following the manufacturing cycle of the PV laminate. A parametric study based on varying interconnect widths is performed. This is followed by an experimental study on the effect of interconnect thickness on the fracture of solar cells during the lamination process. With this knowledge of effect of interconnect geometry on stress distributions developed during the various steps of the manufacturing cycle of a PV laminate, it is hoped that we will be able to design cells which are more resistant to cracking.

2. Structure of a silicon wafer-based photovoltaic laminate and its manufacturing cycle

A typical PV laminate consists of approximately 150 μm-thick silicon solar cells which are connected by copper ribbon interconnects and encapsulated by EVA, glass and polymeric backsheet. These constituent materials protect the mechanical integrity and provide environmental protection of the cells.

The integration process of a PV laminate starts with the soldering of copper ribbon interconnects onto the rear and front sides of the silicon cells at a temperature of approximately 210 °C, the melting point of lead free-solder. It is assumed that the stress state of the entire assembly at this temperature is zero. The interconnected cells are then cooled to room temperature (25 °C) to allow the solder to solidify before proceeding to the next step, lamination. The lamination step consists of stringed cells placed in an assembly of glass, EVA sheets and backsheet. It is placed in a flatbed laminator as illustrated in Fig. 2.

The heating plate is usually set at 150 °C, the curing temperature of EVA. However, studies by Li and Honeker [20,21] have found that placing the laminate immediately onto the table prior to evacuation will cause bowing of the glass sheet at the corners and as a result, non-uniform heating and curing of the EVA. To mitigate this problem, a modified procedure has been suggested where lifting pins are used to elevate the layup above the heating plate to achieve a more uniform preheat. For this study, we shall be focusing on this modified procedure for which the variation of pressure and temperature in the laminator during the lamination process is shown in Fig. 3 below. As such, the lamination process can be further classified into 3 stages.

In the preheating and evacuation stage, the assembly is placed on lifting pins and heated to 50 °C while air in both chambers of the laminator is evacuated. The next step is the pressure-ramping where the assembly is lowered onto the heating plate while the upper chamber is vented. This causes the flexible membrane to apply an atmospheric

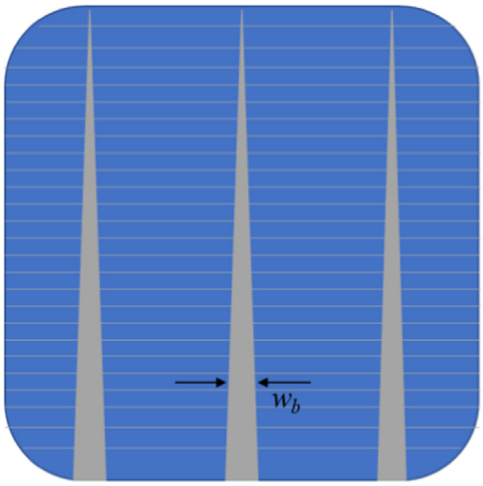

Fig. 1. Design of a width-tapered busbar solar cell [18].

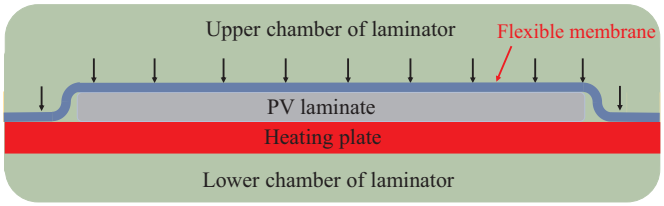

Fig. 2. Cross-section of a lamination chamber (not to scale).