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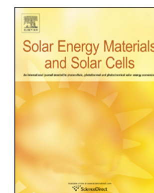
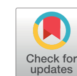


Low temperature growth and extrinsic doping of mono-crystalline and polycrystalline II-VI solar cells by MBE



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ABSTRACT

An investigation of low temperature MBE growth of crystalline $Cd_{(1-x)}Zn_{(x)}Te$ with $0 \leq x \leq 1$, in the range $220\,°C \leq T_s \leq 320\,°C$, and extrinsic doping is conducted. This results in the construction of homo-junction crystalline solar cells on lattice-mismatched 211B and 111B GaAs substrates. Doping and composition studies of crystalline layers are used as a guide for low-temperature, high growth-rate, MBE grown polycrystalline CdTe solar cells on various n-type emitters and different back-contacts. The best resulting devices reach efficiencies of 14.7% under AM 1.5 g, without an anti-reflection coating.

1. Introduction

Most high performance thin-film solar panels on the market today are polycrystalline cadmium telluride (CdTe), a II-VI compound semiconductor. The CdTe absorber is deposited at temperatures above 500 °C via a closed space sublimation or vapor phase transport process onto a window layer of CdS, either sputtered or deposited via chemical bath deposition. The highest efficiency commercial panels are about 16.5% efficient, while the most efficient lab cells have reached an efficiency of about 21.0% [1]. Despite these efficiency achievements, many questions remain about extrinsic doping, deposition temperature, and majority carrier concentration of polycrystalline devices. Copper is typically diffused into the CdTe absorber post deposition since polycrystalline CdTe is hard to dope extrinsically and only a few groups have successfully doped polycrystalline CdTe p-type in situ [2]. However, copper diffusion into the junction region can cause device degradation and is a major source of CdTe cell instability over time [17]. Low doping, in the range of $1–2{\cdot}10^{14}/cm^3$, results in lower open circuit voltages, degraded fill factor, and nearly fully depleted devices unless the absorber layer is thick, i.e., in the range of 5–7 µm. An electron reflector layer such as ZnTe, which is more easily doped p-type, at the back contact can improve this situation, but may contribute to recombination due to defects induced by lattice mismatch at the CdTe/ZnTe interface. In principle, CdTe, with a direct band-gap of 1.5 eV, is an optimal solar absorber for single junction cells, much like GaAs in III-V. GaAs has reached a single junction efficiency of 28.8% with a V_{oc} of 1.12V [3]. However, the best commercial CdTe/CdS devices have V_{oc}'s in the range of 0.8V-0.85 V, although one lab cell has reportedly reached a V_{oc} = 0.9 V with a modified window layer [4].

In this paper, extrinsic doping, dopant concentration, diffusion, and majority carrier concentration in mono-crystalline CdTe, CdZnTe and ZnTe are explored at low substrate temperatures. A low zinc content homo-junction mono-crystalline CdZnTe solar cell is characterized and insights gained are applied to polycrystalline superstrate CdTe/CdS devices deposited at low temperature and high growth-rate on various buffers and TCOs (Transparent Conducting Oxide). The goal is to develop a low temperature deposition process for a wide band-gap solar cell suitable as the top cell of a tandem solar cell. Lattice mismatched substrates were used since any future, economically viable crystalline device will require cheap substrates such as silicon. GaAs is a good substitute since it does not require high-temperature surface preparation. Techniques gleaned from crystalline CdTe and CdZnTe growths were applied to CdTe polycrystalline solar cells since they are benchmarked and relatively well understood. The ability to controllably dope the n-type and p-type layers of the solar cell during growth is key to higher performance and simplified manufacturing. Also, future development of a wide band-gap CdZnTe device may be possible in polycrystalline, where manufacturing techniques are well developed. The initial research described in this paper was divided into two distinct phases. Phase one investigated the in situ doping of cadmium telluride (CdTe), cadmium zinc telluride (CdZnTe) and zinc telluride (ZnTe) mono-crystalline layers grown on lattice mismatched GaAs substrates.

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Crystal growth provides the best way of understanding the doping process because of the easier characterization of the individual layers that make up a solar diode. Phase two utilized the crystalline knowledge as a stepping off point for the growth, composition, and doping of polycrystalline material, whose properties may differ dramatically from crystalline.

2. Methods

All bulk absorber layers referred to in this paper were grown in a Riber 32P MBE with effusion cell sources. Crystalline growth rates were kept to approximately 1 µm/h, while polycrystalline growth rates were as high as 5 µm/h. The limitation on the polycrystalline growths is driven not by any performance limitation requiring slower growth rates, but rather the limited size of the source cells and our maintenance schedule. GaAs and CdZnTe substrates, purchased from WaferTech, LLC and JX Nippon Mining & Metals USA, Inc., respectively, were used for crystalline growths. Semi-insulating (S-I) wafers were used when we required Hall measurements, while conducting substrates allowed vertical VI measurements for diodes. Source material for the MBE effusion cells was 6 N compound ZnTe and CdTe and 6 N elemental Cd, Te, Zn purchased from 5 N Plus Inc. II-VI films were doped p-type using a Nitrogen Plasma source from SVT Associates and n-type using elemental indium and CdCl2 effusion cell materials purchased from Alfa Aesar. An MTI Corporation tube furnace and an in-house gas system were used to anneal samples. Our in-house gas system allows us to perform rapid annealing under a variety of different gas mixtures, including nitrogen, oxygen, argon, and hydrogen. Polycrystalline $CdCl_2$ heat treatments were accomplished in our tube furnace after a final MBE deposition of "cold" (80 °C) $CdCl_2$ onto the sample surface. Typical thicknesses ranged from 100 to 300 nm. Sputtering was performed by a two-gun custom-built sputtering system, NSC-1000, built by Nano-Master Inc. Sputter targets were purchased from ACI Alloys Inc. and Materion. XRD Rocking Curves and SEM were measured at the University of California in Santa Barbara, CA under a facility usage agreement. SIMs measurements were performed by EAG Laboratories.

Hall probe measurements for p-type CdZnTe were made by capping all grown CdZnTe layers with a thin layer of highly doped ZnTe:N. This cap was then selectively etched, leaving only patterned ZnTe corners where good contacts could be made. This technique takes advantage of the fact that the valence band is almost identical from CdTe through CdZnTe to ZnTe providing no impedance to the flow of holes from CdTe or CdZnTe to a highly doped ZnTe contact. Voltage-Current (VI) scans were measured using a calibrated solar tester manufactured by Photo Emissions Technology Inc. incorporating a Keithley 2400 Source Meter.

3. CdTe/CZT crystalline growth on GaAs

Individual CdTe and CdZnTe layers were grown epitaxially on S-I (Semi-Insulating) and p-type GaAs 111B and 211B wafers. GaAs wafers were epi-ready. The wafers were out-gassed by pre-heating in the MBE load lock, under vacuum, at 130 °C for 30 min, and then transferred to the growth chamber. The wafers were heated in the growth chamber and the surface monitored by RHEED (reflection high-energy electron diffraction) as the temperature was raised to deoxidize the surface. At temperatures between 500 °C and 600 °C the RHEED starts to show a bright, well-defined streaky pattern, indicating a two-dimensional crystalline surface ready for the nucleation process. An ω/2θ XRD scan of a GaAs211B substrate produced a baseline 422 peak FWHM of 0.0248°.

It is important to note that there is a 12.5–11.5% lattice mismatch between CdTe or low Zn CdZnTe alloys and GaAs. All CdTe and CdZnTe layers were grown on GaAs with a 1–3 µm CdTe buffer layer with or without an additional thin ZnTe buffer at the GaAs surface to reduce threading dislocations [9]. Growth temperatures were between 220 °C and 320 °C and final thicknesses were between 1 µm and 6 µm.

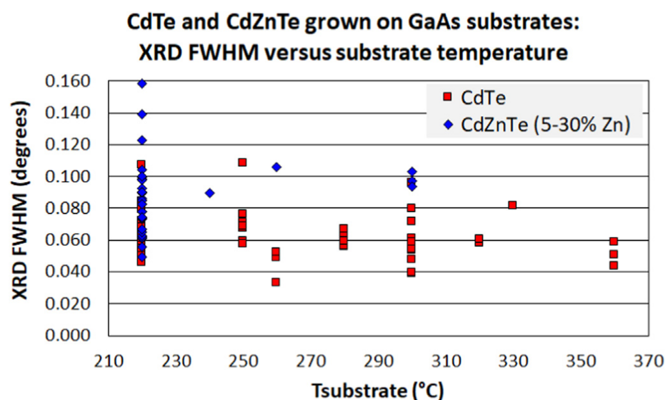

Fig. 1. XRD of CdZnTe and CdTe on GaAs 211B substrates as function of growth temperature.

The Zn content of CdZnTe samples ranged 4% ≤ Zn ≤ 50%; however, those shown in Fig. 1 all have Zn content < 30%. Many of the CdZnTe samples with higher Zn content had FWHM > 0.138°. As is seen in Fig. 1, film quality, as measured by XRD, is fairly uniform across the range of growth temperatures. Variations at different growth temperatures are mainly a function of buffer thickness, with thicker films having smaller FWHM. We found a decreasing density of defects with distance from the lattice mismatched GaAs/(ZnTe)/CdTe interface, leveling off at a thickness d_s = 4–5 µm. At 300 °C, CdZnTe films with d_s ≥ 6 µm have FWHM < 0.0694° [9].

4. *In situ* nitrogen incorporation and diffusion

In an effort to understand in situ nitrogen incorporation in CdZnTe:N, the structure in Fig. 2 was grown on GaAs(211B) at a substrate T_s = 220 °C and constant nitrogen flux:

The SIMs profile is shown in Fig. 2. The middle portion of the CdZnTe growth layers with ~6% Zn content is artificially divided into six 800 nm sections where the sample was turned out of the beam and the temperature was raised to 300 °C at 1 °C/sec and sat for 1 min at 300 °C before cooling down to 220 °C and resuming the growth. This procedure was done to determine the effect of annealing during growth [5]. Fig. 2 shows nitrogen incorporation by the ZnTe and 50% CdZnTe layers is very high at approximately 2.2E19/cm^3 and 1.4E19/cm^3, respectively. The next six regions are demarcated by distinct nitrogen incorporation spikes. For these 6% CdZnTe layers, incorporation of nitrogen ranges from about 3E17/cm^3 to 6E17/cm^3, increasing as the growth moves further away from the original lattice mismatched

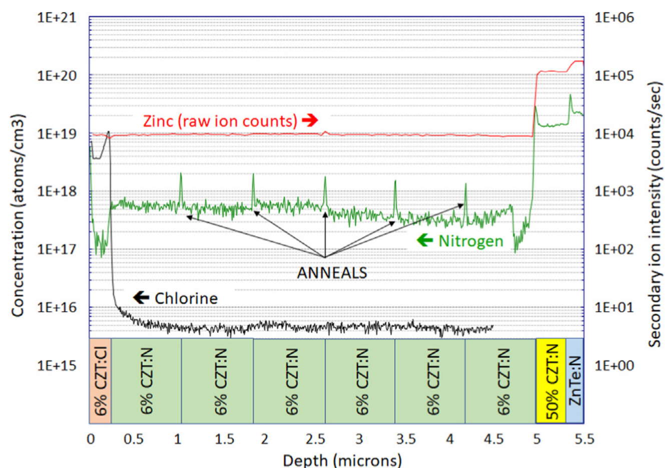

Fig. 2. SIM profile for in situ annealed CdTe:Cl/$Cd_{(1-x)}Zn_{(x)}$Te:N/ZnTe:N/GaAs under constant nitrogen flux and variable zinc content.

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