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Bias and related stress effects in organic thin film transistors based on dinaphtho [2,3-b:2′,3′-f] thieno[3,2-b] thiophene (DNTT)

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ABSTRACT

The effects of bias stress are investigated in organic thin film transistors based on the small molecule dinaphtho [2,3-b:2′,3′-f] thieno[3,2-*b*]thiophene (DNTT) as the semiconductor and polystyrene as the gate insulator, with measurements carried out over a range of temperature and relative humidity. The threshold voltage always shifted in the direction of the applied gate voltage with the effect decreasing as the drain voltage became more negative. In both linear and saturation regimes, the threshold voltage shift followed a stretched exponential dependence on time. Contrary to most previous reports, the threshold voltage after long stress times, asymptotes to a value well below the applied gate voltage. This suggests that the interface trap density in our devices is lower than in previous reports, placing a limit on the shift in flat-band voltage. Bias stress enhances an underlying shift in threshold voltage already caused by increasing relative humidity although under saturation bias stressing the enhancement is minimal. On increasing temperature, bias stress also increases an underlying shift present in the absence of stressing. Stretched exponential fits to the time-decay of drain current indicate an increasing interface trap concentration as temperature increases, but with a shorter trapping time. In all cases, the density of states in DNTT extracted using the Grünewald approach exhibits similar behaviour. As there is no change in the hole mobility, the weak features appearing at the deeper states are unlikely to be related to DNTT. Rather, as the device turns on and the Fermi level at the semiconductor/insulator interface moves down in the bandgap, the flat-band voltage changes in response to changes in electron/hole occupancy of interface states.

1. Introduction

In the last few years, significant progress has been made in developing manufacturing routes for high performance organic electronic circuits. For example, 5-stage ring oscillators operating in the MHz range have been fabricated on pilot line scale using standard lithographic and plasma etching techniques for patterning [1,2]. Similar approaches have been used for fabricating more complex circuits albeit operating at lower frequencies [3,4]. Rapid developments are also being made in manufacturing routes more compatible with roll-to-roll manufacture [5,6]. Developing high-yield manufacturing routes for the reproducible production of high performance circuits is clearly of primary importance. Achieving stable circuit performance over long periods is equally essential and depends on achieving stability at the individual transistor level. Devices must be environmentally stable and especially stable when subjected to electrical stress i.e. bias voltages V_G and V_D applied at the gate and drain respectively, with the source grounded. In α-Si:H thin film transistors, bias stress effects are well-known and have been actively investigated for many decades with a focus on identifying the cause(s) of the threshold voltage, V_T, instability observed during the on-state of the device [7–9]. A similar instability was identified in organic thin film transistors (OTFTs) as early as 1999 [10], albeit on devices formed on inorganic SiO_2 gate dielectrics, and with additional effects arising when an organic dielectric was used [11].

For the period up to 2009, Sirringhaus [12] has reviewed comprehensively the numerous reports published on bias stress in OTFTs and identified a number of common features. For example, negative (positive) gate voltages gave rise to negative (positive) shifts in the threshold voltage resulting from hole (electron) trapping in the semiconductor, at the interface or in the insulator [11,13–18]. Shifts opposite in polarity to the applied gate voltage have also been reported [11], but became less common as improvements in materials and fabrication/measuring conditions reduced the incidences of ionic movement in the gate dielectric. A key focus has been to identify the nature and location of the hole and electron traps in OTFTs. Atmospheric moisture has been identified as the likely source of traps by many researchers [19,20] and several different approaches have been adopted for reducing the ingress

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of moisture. Typically these methods involve (a) passivating the OTFT [21], (b) using self-assembled monolayers to passivate the interface [13,14,22], (c) using hydrophobic dielectrics, such as Cytop™ [23,24], as the gate dielectric and more recently (d) introducing molecular additives to displace water molecules from nanometric pores in the semiconductor [25]. Atmospheric oxygen has also been shown [26], to act as an acceptor-like state trapping electrons when the device is in depletion (off-state) and a donor-like hole trap when the device is in accumulation (on-state).

The time-dependence and extent of the shift in V_T under bias stress has also attracted considerable interest. The stretched exponential function, initially applied to α-Si:H TFTs [7], has also been found to apply to OTFTs [26–30], although the origin of the process is very different - dangling bond creation controlled by hydrogen diffusion in α-Si:H and a dispersive process associated with an exponential distribution of trap energies in OTFTs [12]. Variations have included discrete exponential decays at short times owing to detrapping of electrons but followed by the stretched exponential at longer times [15], simplification to a power-law in time [13], a double stretched-exponential [31,32] and a stretched-hyberbola [19]. In most reports of negative bias stressing of p-type OTFTs, the long-term shift in V_T is generally reported [30] to be such that $(V_G - V_T(\infty)) = 0$, i.e. the gate field becomes insufficient to sustain an accumulation channel of free holes. In some cases, though, the maximum shift in V_T has been limited to ~1 V or less [33,34] by using non-polar dielectrics or SAM layers [35] to avoid the presence of OH groups at the dielectric interface. While most studies concentrate on negative bias stress, positive gate voltages can also result in threshold voltage shifts and has been reported for both metal-insulator-semiconductor (MIS) capacitors [36] as well as in OTFTs [16–18]. The positive voltage shift observed under positive bias stress is generally attributed to injection of electrons into the semiconductor and their subsequent migration to trapping in states at the semiconductor/insulator interface or in the insulator itself. The effect is significantly enhanced under bandgap illumination [37–42] and has also been used to negate the effect of hole trapping under negative bias stress [43,44]. Finally it is worth noting that in many instances [11,15,26,43] bias stress had little or no effect on hole mobility, yet in other cases mobility degradation has been reported [45,46] especially as a result of electron trapping at the interface [47]. Degradation of the subthreshold slope, *SS*, is often observed and has been used to identify a water-related trap in the SiO_2 dielectric [20,48].

Hole mobility in OTFTs based on the small molecule dinaphtho [2,3-b:2′,3′-f] thieno[3,2-*b*]thiophene (DNTT) is typically ~ 1 $cm^2V^{-1}s^{-1}$ but, unlike pentacene, is stable against environmental oxidation. While some studies have been reported on the effect of environmental factors on DNTT OTFTs [35,39,49], studies of bias stress are limited. In one of the few studies [35] it was shown that changes in *SS* could not be reversed on relaxing the device for 1 h after bias stressing for 24 h. In another study [50], stability against bias stress was seen to improve with increasing chain length when a series of alkylphosphonic acids (C_nPA) was vacuum-evaporated onto oxidised aluminium in a two-layer gate dielectric. The improvement was ascribed to better order achieved in the film formed from the longest C_{18}PA molecule. Given that DNTT shows excellent promise for electronic applications, further studies of the bias stress effect are not only highly desirable but also essential. In this contribution, we report the results of bias stress measurements undertaken under a wide range of relative humidity (10% < RH < 60%) and temperature (20 °C < T < 60 °C). Following our recent publication [49], we use the Grünewald approach [51,52] for extracting the semiconductor density of states (DoS) from the transfer characteristics obtained in the linear regime of operation.

Our results lead us to focus attention on the weak features appearing in the DoS in the range 0.2–0.4 eV above the hole transport edge, which we first reported in Ref. [49]. Here we question whether the features are truly representative of DNTT or are a manifestation of a changing interface trap population. We show that, the combination of DNTT and polystyrene (PS) as the dielectric routinely leads to a hole mobility ~ 1 cm^2/Vs that is unaffected by bias stress. Furthermore, the trap density at the DNTT/PS interface is low, so that the long term change in threshold voltage, $\Delta V_T(\infty)$ is much less than generally assumed, i.e. $\Delta V_T(\infty) \ll (V_G\text{-}V_T(0))$ where $V_T(0)$ is the threshold voltage of an unstressed device.

2. Experimental

2.1. Materials and device fabrication

OTFTs based on our previously reported design [5] were fabricated in the bottom-gate, top-contact structure on polyethylene naphthalate (PEN) substrates obtained from DuPont Teijin. Three Kapton® shadow masks (Laser Micromachining Ltd) were used to define features. Firstly, aluminium gate electrodes were evaporated through a shadow mask onto a pre-cleaned PEN substrate. Then the gate dielectric, polystyrene (Sigma Aldrich, M_W = 350,000), was spin-coated from 8 wt% toluene solution and heated for 10 min at 100 °C to remove residual solvent. The resulting film, typically 1 μm thick had a capacitance per unit area, C_i = 2.37 nF/cm^2. DNTT, synthesised and purified at Manchester University, was evaporated to a thickness of 60 nm through a second shadow mask. Finally, gold source/drain electrodes were evaporated through a third mask to define channels of width, W = 2 mm and lengths, L = 150 μm or 200 μm. In keeping with earlier findings [5], prior to undertaking any measurements, devices were left exposed to laboratory air for 48 h to achieve optimum performance.

2.2. Bias stress measurements

Transistor output (I_D-V_D) and transfer (I_D-V_G) characteristics were measured using a Keithley source-measure unit (model 2636B). Initial measurements were carried out with devices located in an earthed metal box in a laboratory environment (T ~ 20 °C, 40% < RH < 60%). In later measurements, devices were exposed to controlled temperature and relative humidity, again in the dark, but now in an Environmental Chamber (Climacell). Prior to applying bias stress, initial output and transfer characteristics were measured. Devices were then subjected to various bias stress voltages for increasing lengths of times with the stress being interrupted periodically to re-measure the output and transfer characteristics. The effects of bias stress were quantified by noting changes in parameters extracted from transfer characteristics, namely turn-on voltage, V_{ON}, threshold voltage, V_T, mobility, μ, and subthreshold slope, *SS*. In this work, V_{ON} is defined as the voltage at which the channel current exceeds the off-current which, for an intrinsic semiconductor, is approximately equal to the flat-band voltage, V_{FB}. (In our case, the true off-current is less than the displacement current, ~10 pA, generated during the gate voltage sweep). We take V_T to be the intercept on the voltage axis when extrapolating the linear sections of I_D-V_G plots in the linear and $I_D^{1/2}$-V_G plots in the saturation regimes. The gate-voltage-dependence of the hole mobility was also extracted from transfer plots in the linear and saturation regimes respectively using standard equations [53] i.e.

$$\mu_{lin} = \frac{L}{WC_iV_D}\cdot\frac{\partial I_D}{\partial V_G} \quad (1)$$

and

$$\mu_{sat} = \frac{2L}{WC_i}\cdot\left(\frac{\sqrt{\partial I_D}}{\partial V_G}\right)^2 \quad (2)$$

The subthreshold slope, *SS,* was extracted over the range of V_G corresponding to 10 pA ≤ I_D ≤ 100 pA using the relation

$$SS = \frac{\partial V_G}{\partial(\log I_D)} \quad (3)$$

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