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Improved SOI LDMOS performance by using a partial stepped polysilicon layer as the buried layer

Jingwei Guo, Shengdong Hu*, Ye Huang, Qi Yuan, Dong Yang, Ling Yang, Liang You, Jianyi Yu

Key Laboratory of Dependable Service Computing in Cyber Physical Society, Ministry of Education, and Chongqing Engineering Laboratory of High Performance Integrated Circuits, College of Communication Engineering, Chongqing University, Chongqing 400044, China

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ABSTRACT

A novel SOI LDMOS with a stepped polysilicon compound buried layer (SP-CBL) is proposed in this paper. In the SP-CBL SOI LDMOS, a stepped polysilicon layer is introduced into the buried layer. Firstly, SP-CBL brings in two new electric field peaks and modulates the electric field of drift region and obviously promotes the breakdown voltage (*BV*). Secondly, SP-CBL reduces the thickness of the top buried oxide layer, and the doping concentration of the drift region is thus increased according to the RESURF condition. The specific on-resistance ($R_{on,sp}$) is reduced. In addition, the polysilicon conducts heat more efficiently than SiO_2, relieving the self-heating effect to some extent. The effects of critical structure parameters on the device performances are investigated. Ultimately, compared with the partial compound buried layer structure (P-CBL SOI LDMOS), *BV* of SP-CBL SOI LDMOS is enhanced by 13.7% and $R_{on,sp}$ is reduced by 15% at the same device dimension, and the maximum temperature is dropped by 7.2 K at the power of 1 mW/μm. Compared with the conventional SOI LDMOS (C-SOI LDMOS), *BV* is enhanced by 66.3%, $R_{on,sp}$ is reduced by 52.4%, and temperature is depressed by 11.4 K.

1. Introduction

As one of currently mainstream technology in semiconductor field, Silicon-On-Insulator (SOI) technology is often applied into LDMOS [1–3]. In this way, device not only has the advantages of SOI such as high speed and gain, favorable linearity, fast frequency and low loss, but also inherits the characteristics of good horizontal mobility and high process compatibility from LDMOS [4–8]. The ultimate goal of designing the kind of SOI LDMOS is to keep a trade-off between the breakdown voltage (*BV*) and the specific on-resistance ($R_{on,sp}$) [9,10]. Many techniques have been proposed to accomplish this trade-off, such as reduced surface field (RESURF) [11–14],variable doping profile technology [15,16],enhanced dielectric layer field [17,18], and so on [19–22]. Compound buried layer (CBL) structure was proposed to obviously relieve the trade-off between *BV* and $R_{on,sp}$, which also improved the thermal performance [23,24].

In this paper, the stepped polysilicon layer inserted into buried layer of SOI LDMOS is presented and the influence of the polysilicon layer is investigated. In the SP-CBL LDMOS, the stepped compound buried layer replaces the buried oxide layer under the source-side, which is able to optimize the surface electric field and obtain a higher *BV*. Meanwhile, the introduction of SP-CBL improves the doping concentration of drift region, leading to a lower $R_{on,sp}$. Moreover, the SP-CBL also improves thermal performance. More details and the influence of device structure parameters are investigated in next chapter.

2. Structure and mechanism

Fig. 1 shows the schematic cross-section of the novel SP-CBL SOI LDMOS, partial compound buried layer structure SOI LDMOS and conventional SOI LDMOS, respectively. As seen in the Fig. 1(a), a stepped polysilicon compound buried layer is inserted into the buried oxide layer of device. According to the expression of $V_{B,V} = 0.5E_{si}t_{si} + E_{ox}t_{ox}$, where E_{ox} and E_{si} are the interface vertical electric fields in oxide and silicon. Since the maximum vertical electric filed is under the drain for the LDMOS, to avoiding a low $V_{B,V}$ created by a thin t_{ox}, SP-CBL is placed under the source [23]. t_{Si} and t_{cbl} (t_{ox}) are thickness of top silicon layer and overall buried oxide layer, respectively. t_{ox1} and t_{ox2} represent the thickness of top oxide layer and bottom oxide layer. L_{step} and t_{step} are the length and thickness of stepped polysilicon layer, respectively. L_{drf} and N_{drf} are the length and doping concentration of drift region. Two-dimensional device simulator MEDICI is used in this paper to study the mechanism of the devices. The physical models including CONSRH, AUGER, CONMOB and FLDMOB are used in the simulation and the NEWTON solution method is carried out with 2 types of carriers. The key device structure parameters are given in the

* Corresponding author.
E-mail address: hushengdong@hotmail.com (S. Hu).

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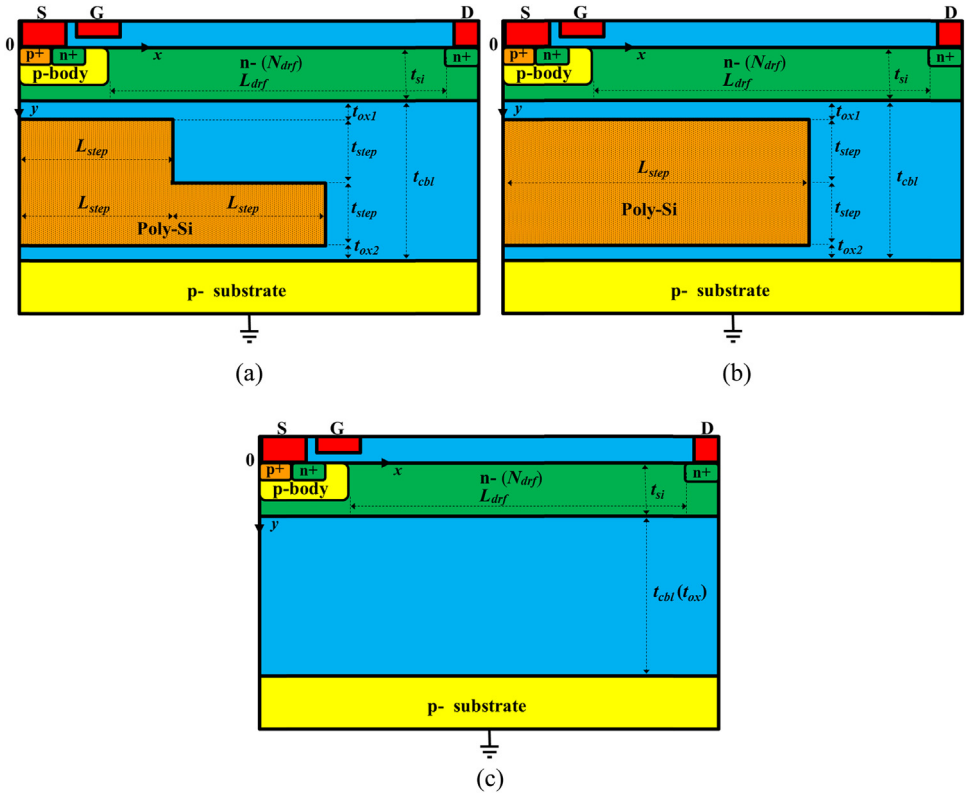

Fig. 1. Schematic diagrams of (a) SP-CBL SOI LDMOS, (b) P-CBL SOI LDMOS and (c) C-SOI LDMOS.

Table 1
Device parameters used in the simulation.

Device parameters	SP-CBL SOI	P-CBL SOI	C-SOI
Length of drift region, L_{drf} (μm)	48–64	48–64	48–64
Length of stepped polysilicon layer, L_{step} (μm)	16–21.3	16–21.3	–
Thickness of top silicon layer, t_{si} (μm)	2	2	2
Thickness of buried oxide layer, t_{cbl} (μm)	6.3	6.3	6.3
Thickness of p-substrate layer, t_{sub} (μm)	2	2	2
Thickness of top oxide layer, t_{ox1} (μm)	Optimized	Optimized	–
Thickness of middle stepped polysilicon layer, t_{step} (μm)	2.45–2.25	4.2–4	–
Thickness of bottom oxide layer, t_{ox2} (μm)	0.3	0.3	–
n-type doping concentration in drift region, N_{drf} (cm^{-3})	Optimized	Optimized	Optimized
p-substrate concentration, P_{sub} (cm^{-3})	8×10^{14}	8×10^{14}	8×10^{14}

Table 1.

According to the RESURF condition of the SOI device, when the device reaches its maximum breakdown voltage, the drift region must have been completely depleted. That's to say, the product of net charge quantity in drift region and buried oxide layer characteristic thickness (t) has to be limited to a certain range as $t = \sqrt{0.5t_{si}^2 + (\varepsilon_{si}/\varepsilon_{bl})t_{si}t_{bl}}$ [25], where ε_{si} and ε_{bl} are the permittivities of silicon and buried layer, and t_{bl} is the thickness of the buried layer. Generally, when drift region is doped uniformly and t is fixed, then the net charge concentration is also fixed. While the introduction of stepped buried polysilicon layer creates a stepped buried oxide layer structure for SP-CBL LDMOS, which consists of three parts of different t from the source to the drain. So three regions with different buried oxide layer characteristic thicknesses are formed, which meet different RESURF conditions. The insertion of SP-CBL introduces two new electric field peaks at the corners of stepped buried polysilicon. Firstly, the introduction of new electric field peaks optimizes the lateral electric field distribution of the drift region, leading to an enhanced the lateral breakdown voltage (V_{BL}). Secondly, on the basis of SOI RESURF condition, thinner buried oxide layer will lead to higher optimal N_{drf}. Compared with two other devices, SP-CBL SOI LDMOS owes buried oxide layer with smaller thickness, which means the N_{drf} of SP-CBL SOI LDMOS is higher. Then, on the one hand, higher N_{drf} leads to lower $R_{on,sp}$. On the other hand, the electric field at the interface between top silicon and buried oxide layer is enhanced owing to a higher N_{drf}, which results in a higher vertical breakdown voltage (V_{BV}). Therefore, the SP-CBL SOI LDMOS can effectively improves the tradeoff between BV and $R_{on,sp}$. Finally, the thermal conductivity of polysilicon is much higher than that of SiO_2 of SP-CBL SOI LDMOS, due to which the self-heating effect is significantly improved.

3. Result and discussion

3.1. Off-state

Fig. 2 shows the equipotential contours at breakdown for SP-CBL SOI LDMOS, P-CBL SOI LDMOS and C-SOI LDMOS. Compared with the C-SOI LDMOS, the equipotential contours distributions of the SP-CBL SOI LDMOS and the P-CBL SOI LDMOS are more uniform and denser. It can be seen that SP-CBL SOI LDMOS and P-CBL SOI LDMOS introduce more equipotential contours in the middle of the drift region especially at the corners of polysilicon layer.

Fig. 3 gives schematic shows the electric fields distributions at breakdown for SP-CBL, P-CBL and C-SOI LDMOS, respectively. Fig. 3(a) is the lateral electric field distributions of three devices, because of the modulation effect caused by the inserted stepped polysilicon buried layer, two new peaks (point O and point P) are introduced into SP-CBL SOI LDMOS, which is different with P-CBL SOI LDMOS and C-SOI LDMOS. It can be seen clearly that the SP-CBL SOI LDMOS owes a higher interface electric field peak and a lower surface electric field peak than P-CBL SOI LDMOS. Fig. 3(b) is the vertical electric field distributions under the drain side. Compared with two other devices, the electric field in buried oxide layer(2–8 μm) of SP-CBL SOI LDMOS is