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Study of SiC buffer layer thickness influence on photovoltaic properties of n-GaN NWs/SiC/p-Si heterostructure

K.Yu. Shugurov[a], R.R. Reznik[b], A.M. Mozharov[a], K.P. Kotlyar[a], O.Yu. Koval[a], A.V. Osipov[a,d], V.V. Fedorov[a], I.V. Shtrom[c], A.D. Bolshakov[a], S.A. Kukushkin[a,d], I.S. Mukhin[a,b,*], G.E. Cirlin[a,b,c]

[a] St.Petersburg Academic University, 194021 St. Petersburg, Russia
[b] ITMO University, 197101 St. Petersburg, Russia
[c] Institute for Analytical Instrumentation RAS, 190103 St. Petersburg, Russia
[d] Institute of Problems of Mechanical Engineering RAS, 199178 St. Petersburg, Russia

ABSTRACT

In this paper we study the solar cell based on GaN nanowires array grown on Si substrate with buffer SiC layer via molecular beam epitaxy. Crystal quality of SiC layer and GaN nanowires was studied by means of Raman scattering technique and low temperature photoluminescence measurements. Spectral and volt-ampere characteristics of the n-GaN/SiC/p-Si heterostructures with different thickness of diffusive buffer SiC-3C layers were studied. It was shown that increase of the buffer layer thickness over 100 nm leads to rise of the open circuit voltage and to increase of the efficiency of solar cell in comparison with n-GaN/p-Si heterostructure without buffer layer. Experimental data shows the presence of the defect states at the heterointerface.

1. Introduction

Integration of III-V semiconductors with Si platform is the topical problem of modern science and technology. III-V semiconductor materials such as GaAs, InP, and (Al, Ga, In)N possess direct band gap structure and high electron mobility making them very promising for development of functional structures for efficient light emitting diodes, high power transistors, microwave signal generators and photoactive layers of solar cells (SCs). It is well known, that the optoelectronic device characteristics are mainly governed by the crystalline quality of the grown semiconductor structure. The best results can be achieved with the use of substrates lattice-matched to the synthesized semiconductor layers. Low cost, excellent thermal conductivity and mechanical properties as well as well-developed Si post-growth technologies make Si substrates very attractive from the device application point of view. On the other hand, large lattice mismatch of Si with most of the III-Vs limits development of functional III-V heterostructures synthesized on Si substrates.

III-N semiconductors and their solid solutions are well-established materials for development of light emitting diodes and SCs [1,2]. The major factor limiting growth of III-N based devices production is the lack of inexpensive substrates lattice-matched to III-N materials. The most important from technological point of view and the most studied material among the III-Vs is GaN. Conventionally sapphire and SiC substrates having sufficient mismatch with III-N materials are used for GaN synthesis [3]. Lattice mismatch of Si with GaN (17%) and the thermal expansion coefficient mismatch (55.7%) lead to appearance of dislocations penetrating the entire GaN/Si heterostructure resulting in the deterioration of the device characteristics.

Due to a large lattice mismatch, epitaxial GaN normally grows on Si substrate in the shape of columnar structures also known as nanowires (NWs) with wurtzite crystal lattice typical for this material in bulk. Due to the large area sidewalls of the NWs, the elastic mechanical strain of the lattice relaxes effectively during the structure growth, and the grown NWs have high crystalline quality. Vertically aligned arrays of NWs, possessing unique properties, are potential building blocks for optoelectronic devices, in particular solar cells [4]. Advantages of these nanostructures use in the field of photovoltaics are associated with low material consumption and possibility to improve light trapping through optimization of the nanostructure morphology [5,6]. It should be mentioned that quasi one-dimensional geometry of the NWs provides good transport properties of photogenerated carriers and may significantly reduce recombination losses [7,8]. In our previous work [2] the SCs based on the n-GaN NWs synthesized on p-Si substrate with efficiency exceeding 20% was considered and studied theoretically.

Despite the fact that GaN crystal quality issue can be overcome with the growth of NWs on Si, the problem of mutual doping occurs due to the relatively high growth temperatures, and consequently, enhanced bulk diffusion of the impurities [9–11].

Typical duration of GaN NWs growth on Si substrate in case of

* Corresponding author.
E-mail addresses: imukhin@yandex.ru, imukhin@spbau.ru (I.S. Mukhin).

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molecular beam epitaxy (MBE) is several hours and the temperature value is 800 °C. Considering Ga bulk diffusion coefficient in Si in the order of 3×10^{-17} cm^2/s [12] the calculated value of Ga impurities in Si at the distance of several tens of nanometer from the substrate surface can reach the value corresponding to the doping level at the heterointerface. Actual concentration will be limited with the impurity solubility limit at given temperature and in our case would not exceed 10^{19} cm^{-3} [12]. Presence of metal atoms in Si decreases the minority carriers' lifetime dramatically affecting the photovoltaic properties of the GaN/Si heterojunction.

It is well known, that growth of GaN on Si surface is accompanied with formation of a thin SiN layer [9]. The thickness of this layer is limited with the bulk diffusion of nitrogen atoms into Si substrate [13] and in SiN layer itself [14] and cannot exceed few monolayers at the given temperature. With this thickness SiN layer does not suppress Ga diffusion into the substrate.

In order to reduce the discussed effects, the layers suppressing the mutual diffusion of impurities can be used. An example of the effective diffusion barrier at the GaN/Si heterointerface is SiC [14]. During development of GaN/SiC/Si heterostructure SC we have to consider influence of SiC layer on electronic properties of the rectifying junction. Analysis of the structure band diagram shows that the use of SiC-3C layer sufficiently affects the SC characteristics. Use of undoped SiC-6H leads to emergence of the barrier for electrons between Si and GaN reducing the current and consequently efficiency of the structure.

In papers [15,16] the I-V curves of the p-SiC/p-Si and n-SiC/p-Si heterojunctions with 3C-SiC layers formed with low pressure chemical vapor deposition (LPCVD) method on Si substrates were obtained and analyzed. To describe the curves the authors used the experimental values of the bands misalignment [17]. It was demonstrated, that the junctions provide rectifying behavior persistent to high temperature annealing and mechanical strains.

In our work we have studied p-Si/i-SiC/n-GaN NWs heterostructures with undoped SiC buffer formed via Si atoms substitution [18–20]. The operating modes of the SCs with different thickness of SiC layers were studied experimentally.

2. Experimental

2.1. SiC buffer layer synthesis

Formation of the SiC buffer layer on Si (111) substrate was performed along the method described in [18–20]. This method differs from all of the currently existing epitaxial methods and technologies for the single crystals, films and nanostructures growth. Briefly, the method is based on the substitution of Si atoms with carbon ones in the substrate. At the first stage, carbon atom is embedded into interstitial site of Si. Then, the nearby Si atom is removed forming a Si vacancy. As a result, at the surface the dilatation dipoles are created (stable complexes consisting of dilatation centers — the Si vacancy and a C atom in interstitial site). These two centers elastically interact with each other in crystal of cubic symmetry. The chemical reaction rate is the most efficient in the direction along attraction of dilatation dipoles (i.e. along the (111) direction in the substrate). Orientation of the film depends on the crystal structure of the original Si matrix, not only the substrate surface, as typically used in conventional film growth techniques. The temperature and pressure of the gas are selected to nucleate SiC. Formation of the elastic dipoles (C atom — Si vacancy) provides high quality SiC film formation.

As follows from the growth process description, the source of Si atoms to form SiC layer is the wafer. Due to significant amount of Si atoms required for the formation of the SiC layer the porous structure is formed underneath the SiC layer. To form thicker SiC layers more Si is needed leading to higher porosity observed in thicker SiC layers.

This method allows formation of high crystal quality SiC layers and is much cheaper in comparison to the conventional epitaxial methods. The main drawback of the method is the formation of the voids in Si substrate under the SiC layer leading to high density of the electronic states at the interface acting as recombination centers and, consequently, leading to deterioration of the junction rectifying behavior and to high density of the leakage current with reverse bias.

In order to carry out comprehensive study of SiC influence on photovoltaic properties of n-GaN/SiC-3C/p-Si heterostructure we have fabricated the samples with 50 nm, 100 nm, 150 nm thick SiC buffer layers and without the latter.

2.2. MBE synthesis of the heterostructures

The samples with n-GaN NWs were synthesized via plasma-assisted MBE deposition in Riber 12 Compact machine equipped with a Ga effusion cell, plasma activated nitrogen source and Si doping cell. P-type Si (111) wafers were used as substrates. The growth conditions for all of the samples were identical. First, the substrate temperature was set to 950 °C for thermal treatment in the growth chamber. Then the substrate temperature was lowered to the growth value of 880 °C, the nitrogen plasma source was ignited and set to 1.5 sccm flux and 520 W for plasma source power. Finally, the Ga source was opened. The Ga flux was set at $1.1 \cdot 10^{-7}$ Torr as was measured with Bayard-Alpert gauge prior to the growth. The growth rate for Ga was set at 0.01 ML/s (according to the calibrations) to ensure nitrogen-stabilized growth conditions allowing to synthesize the NWs [21]. The total growth time was 15 h. The NWs growth was monitored in situ using reflection high energy electron diffraction (RHEED) demonstrating pure wurtzite structure of the NWs after incubation period (see insert in Fig. 1). According to the RHEED pattern monitoring, the incubation time was only several seconds. On the contrary, GaN NWs incubation period on Si substrate usually takes more than ten minutes. Since the growth of the NWs was carried out at elevated temperature (in comparison with growth on Si substrate), Ga atoms sticking probability on SiC layer was rather small and the growth of the NWs was selective without formation of planar GaN layer between them. In fact, we have never observed this layer appearance for the growth of GaN on SiC under the similar growth conditions (nitrogen-stabilized conditions and elevated temperatures).

Scanning electron microscopy (SEM) images of the GaN NW arrays and GaN/SiC/Si heterointerfaces with different SiC thickness layers are presented in Fig. 1. As can be seen from the figure very dense arrays of irregularly shaped vertical NWs were obtained.

Data on GaN NWs array and SiC buffer layer morphology for all of the studied samples is presented in Table 1.

2.3. Solar cell processing

The post-growth methods were used for fabrication of ohmic contacts and further development of the SC prototypes. On the first step, aluminum layer was deposited on the back side of the sample via vacuum thermal deposition. The rapid thermal annealing was then used to obtain ohmic back contact. Next, the dielectric epoxy layer was deposited on the top surface of the sample followed by unsheathe of the NWs top grains via etching in oxygen plasma precisely ex-situ controlled with SEM. On the next step, transparent contact ITO layer in the shape of 2.5 mm circle mesa was deposited through metallic mask on the top surface of the heterostructure. The contact bars made of conducting silver paste were fabricated at the last stage. Shadowing of the mesa photoactive region with the bars did not exceed 2%.

2.4. Spectral and electrical characteristics measurement

Structural characteristics of the synthesized GaN/SiC/Si heterostructure were investigated with Raman scattering technique. The measurements were performed at room temperature in backscattering geometry with a 532 nm Nd: YAG laser excitation at normal incidence (along the c-axis of GaN) with the use of Horiba Jobin-Yvon LabRam