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Impact of remote oxygen scavenging on the interfacial characteristics of atomic layer deposited $LaAlO_3$

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In this paper, the influence of a remote interfacial layer (IL) scavenging method on the interfacial characteristics of $LaAlO_3$ grown by atomic layer deposition (ALD) on Si substrates has been studied. After the fabrication of Pt/$LaAlO_3$/Si and Pt/Ti/TiN/$LaAlO_3$/Si metal-insulator-semiconductor (MIS) capacitors, the microstructures and electrical properties of these MIS capacitors have been comparatively investigated. High resolution transmission electron microscopy (HRTEM) analysis shows that the thickness of IL between $LaAlO_3$ films and Si substrates is reduced by remote IL scavenging technique, contributing to lower equivalent oxide thickness (EOT) and to higher dielectric constant values. However, larger amount of oxygen vacancies and dangling bonds are induced in the MIS structure with IL scavenging reaction, resulting in a slight degradation of the gate leakage current-voltage and the breakdown characteristics.

1. Introduction

With the successive scaling of metal oxide semiconductor field effect transistors (MOSFETs), traditional SiO_2 dielectrics are gradually substituted by high dielectric constant (high-k) materials (e.g., HfO_2) [1]. Unfortunately, the formation of interfacial layers (ILs) between high-k materials and silicon substrates with low permittivity is unavoidable, which will impede further equivalent oxide thickness (EOT) scaling [2]. In order to get lower EOT, there are two commonly used methods. One is reducing the thickness of the IL, and the other is introducing a new kind of high-k material with higher permittivity value. Recently, the remote IL scavenging technique has been considered as one of the most effectual methods in EOT scaling, which could enable EOT scaling below 0.5 nm in the HfO_2-based high-k gate dielectrics and metal gate electrodes (HKMG) structures [3] by a cascade reaction of oxygen transfer from the IL to the metal layer (e.g., Ti) with the help of oxygen vacancies in the dielectric film [4]. However, the aggressive EOT scaling of HfO_2 is limited by its k-value (~20), implying that the dilemmas of EOT scaling in HfO_2 will not be completely solved even after using the scavenging technique. Thus, replacing HfO_2 with materials with k values greater than 20 is considered as a long term scaling solution. Owing to the high k value of ~25, large band gap (~6.2 eV), and excellent thermal stability, La-based oxides have been considered as a promising gate dielectric in silicon-based MOSFETs [5]. However, due to the high affinity of La-based oxides with Si atoms, a thicker IL will form when La-based films are deposited on Si substrates without any surface passivation treatment, which will further impede the EOT scaling [6]. Besides, the hygroscopicity of La_2O_3 dielectric also limits its application as gate oxides in MOSFETs. Previous studies have shown that $LaAlO_3$ (LAO), as a compound of La_2O_3 and Al_2O_3, has nearly the same dielectric constant as La_2O_3 while offering both high immunity against moisture and great suppression of Si out-diffusion effects [7]. But in recent years, the remote IL scavenging technology based on HfO_2 has been extensively studied, while few researches have focused on the effects of the remote IL scavenging on La-based high-k dielectrics.

In this paper, a remote IL scavenging method for reducing the SiO_x-based IL thickness after the deposition of $LaAlO_3$ on Si substrates was investigated. Attention was focused on the impacts of this IL scavenging method on interfacial issues of $LaAlO_3$/Si structures.

2. Experiment

2 in. P-type Si (100) wafers with resistivity of 3–8 Ω cm were treated by stress relieved pre-oxide (SRPO) [8], i.e., SiO_2 was grown on the RCA cleaned Si surface in oxygen at 1000 °C for 45 s, then, the thermally grown SiO_2 was removed by the diluted HF solution. After substrate pretreatment, the temperature of the Picosun R-150 ALD reactor was set as 300 °C, and ~5 nm $LaAlO_3$ (La/Al ratio as 2:1) thin films were deposited on the wafer. $La(^{i}PrCp)_3$ and $Al(CH_3)_3$ were used as La and Al precursors (both are provided by J&K Scientific LTD), and O_3

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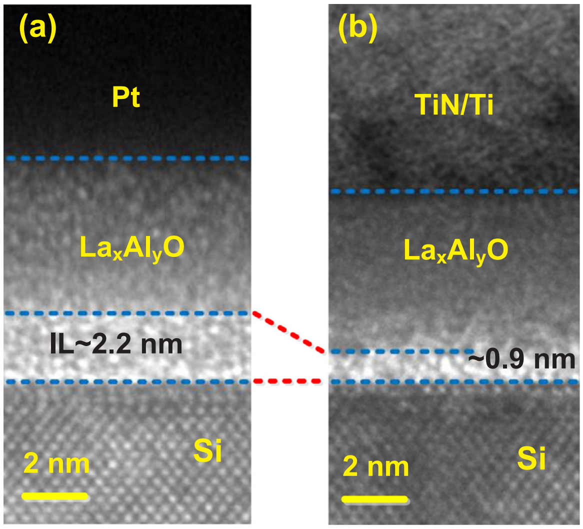

Fig. 1. HRTEM images for the samples S1 (a) and S2 (b).

was used as oxidant. Post-deposition annealing (PDA) was carried out soon after film deposition in vacuum at 600 °C for 60 s. Later, 100 nm Pt and 2 nm TiN/5 nm Ti/100 nm Pt metal gates with a diameter of 300 µm were prepared by using electron-beam evaporation through a shadow mask. After the back contact metal Al was sputtered, the samples were treated in forming gas (97% N_2/3% H_2) at 400 °C for 20 min. For simplicity, samples using 100 nm Pt and 2 nm TiN/5 nm Ti/100 nm Pt as gate electrodes were assigned as S1 and S2, respectively.

Cross-sectional high resolution transmission electron microscopy (HRTEM) was performed to measure the film thickness and to observe the microstructures of the fabricated nanolaminates. The electrical properties of the samples, including capacitance-voltage (*C-V*), conductance-voltage (*G-V*), leakage current density-voltage (*J-V*) and time-dependent dielectric breakdown (TDDB) characteristics, were measured using an Agilent B1500A semiconductor parameter analyzer.

3. Results and discussion

The cross-sectional HRTEM images for samples S1 (a) and S2 (b) are shown in Fig. 1. Compared with Fig. 1(a) in which an amorphous IL (~2.2 nm) between the deposited La_xAl_yO film and Si substrates is observed, a much thinned IL (~0.9 nm) exists at the layer interface in Fig. 1(b). These structural differences are mainly related to the TiN/Ti metal gate. At room temperature or annealing temperature, the negative Gibbs free energy can only be obtained from the first two reactions in Table 1, which means the Gibbs free energy of Ti is much lower than that of Al and La but larger than that of Si, indicating that Ti can only scavenge O atoms from SiO_x-like compounds in the IL [9]. Thus, using TiN/Ti/Pt instead of Pt as the gate electrode will effectively reduce the thickness of the IL between silicon substrates and $LaAlO_3$ films by scavenging oxygen from IL. However, as shown in Fig. 1(b), the sample S2 treated with remote oxygen scavenging still preserves about 0.9 nm IL, which can be explained by the following two reasons. On the one hand, even though the O atoms can be adsorbed by Ti metals, the scavenging capability of Ti is limited; On the other hand, the SRPO process has strengthen the chemical bonds between ILs and substrates, resulting in the weakening of the remote oxygen scavenging effect [10].

Table 1
Change in Gibbs free energy for possible oxidation reactions of Ti [11].

Reaction	ΔG (kJ/mol) at 298 K	ΔG (kJ/mol) at 873 K
$Ti + SiO_2 \rightarrow TiO_2 + Si$	− 39.3822	− 51.1179
$Ti + 3/4SiO_2 \rightarrow 1/2Ti_2O_3 + 3/4Si$	− 80.1256	− 85.3366
$Ti + 2/3Al_2O_3 \rightarrow TiO_2 + 4/3Al$	166.0747	152.4549
$Ti + 1/2Al_2O_3 \rightarrow 1/2Ti_2O_3 + Al$	73.96704	67.34304
$Ti + 2/3La_2O_3 \rightarrow TiO_2 + 4/3La$	248.5558	242.2959
$Ti + 1/2La_2O_3 \rightarrow 1/2Ti_2O_3 + La$	135.8278	134.7238

The *C-V* and *G-V* characteristics of the two samples (S1 and S2) are shown in Fig. 2. The gate voltage is swept from positive to negative (+3 V to -3V) and swept back from negative to positive (-3V to +3 V) at the frequency of 100 kHz to obtain the *C-V* hysteresis. When the *C-V* hysteresis is measured from +3 V to -3V, the *G-V* characteristics are also measured synchronously. Using NCSU CVC program [12], the EOT values of the fabricated MIS capacitors S1 and S2 are obtained to be 2.69 nm and 1.71 nm, respectively. And the relative dielectric constant of high-k dielectric ($k_{high\text{-}k}$) of S1 and S2 are calculated to be 9.7 and 12.5, through the following commonly used formula:

$$k_{high-k} = \frac{\varepsilon_{SiO_2}}{EOT} t_{high-k} \quad (1)$$

where $t_{high\text{-}k}$ is the thickness of high-k dielectric film, the $t_{high\text{-}k}$ values of S1 and S2 are extracted to be 6.7 nm and 5.5 nm from the HRTEM images; ε_{SiO2} is the relative dielectric constant of SiO_2, and the commonly used value is 3.9. Compared with S1, the EOT value of S2 has decreased by 1 nm, while the $k_{high\text{-}k}$ value has increased by 3, which confirms that the IL thickness between $LaAlO_3$ layer and Si substrate is indeed reduced by the remote oxygen scavenging method in sample S2, coinciding with the results of HRTEM analysis.

Although the flat band voltages (V_{FB}) of the two samples vary greatly in *C-V* curves, it is meaningless to compare the V_{FB} differences since two kinds of metal electrodes were used. By observing Fig. 2(a), the forward and backward *C-V* curves of S2 almost overlap with each other in the weak inversion region. In Fig. 2(b), a small hysteresis appears in the weak inversion region of *C-V* hysteresis curves. Numerous reports have demonstrated that the characteristics of hysteresis in *C-V* curves depend on oxide trapped charges (Q_{ot}) [13]. Thus, the different degrees of hysteresis in Fig. 2 indicate that larger amount of Q_{ot} are brought in the $LaAlO_3$ layer of $Pt/Ti/TiN/LaAlO_3/Si$ MIS capacitors by the remote oxygen scavenging method.

Fig. 3 records *C-V* characteristics at various frequencies (1 kHz–1 MHz) of the fabricated MIS capacitors S1 (a) and S2 (b). As shown in Fig. 3, the multi-frequency *C-V* curves of sample S2 show more serious frequency dispersion in the weak inversion region and accumulation region. It is reported that the anomalous hump phenomenon in weak inversion region is associated with the formation of interface trapped charges (Q_{it}) originating from the faster capture and emission of carriers [14], and the frequency dispersion in accumulation region is attributed to the frequency-dependent changes in the dielectric constant caused by oxygen vacancies in the gate stacks [15]. Therefore, it can be qualitatively said that larger amount of Q_{it} and oxygen vacancies exist nearby the IL of the fabricated MIS capacitor S2 compared with S1.

In addition, the various electrical parameters of mentioned above, such as oxide trapped charges density (N_{ot}) and interface trapped charges density (D_{it}), can be acquired by the following equations [16,17]:

$$N_{ot} = \frac{\Delta V_{FB} C_{ox}}{qA} \quad (2)$$

$$D_{it} = \frac{2}{qA} \frac{\frac{G_{max}}{\omega}}{\left[\left(\frac{G_{max}}{\omega C_{ox}}\right)^2 + \left(1 - \frac{C_{max}}{C_{ox}}\right)^2\right]} \quad (3)$$

where C_{ox} is the accumulation capacitance, ΔV_{FB} is the hysteresis width, A is the electrode area, q is the electron charge, ω is the angular frequency, C_{ac} is the measured accumulation capacitance, G_{ac} is the conductance in accumulation region, G_{max} is the maximum value of *G-V* curve, and C_{max} is the corresponding capacitance of the gate voltage at which the G_{max} is obtained. Therefore, for the sample S1 and S2, the