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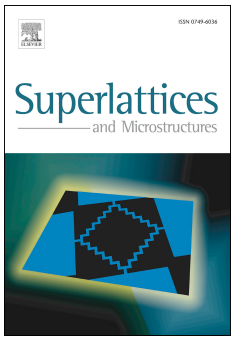

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PII: S0749-6036(18)31078-4

DOI: 10.1016/j.spmi.2018.07.038

Reference: YSPMI 5842

To appear in: *Superlattices and Microstructures*

Received Date: 22 May 2018

Revised Date: 28 July 2018

Accepted Date: 28 July 2018

Please cite this article as: L. Wu, Y. Zhang, H. Yang, Y. Song, N. Yuan, B. Lei, L. Hu, Y. Wu, Optimization of novel superjunction LDMOS with partial low K layer, *Superlattices and Microstructures* (2018), doi: 10.1016/j.spmi.2018.07.038.

Optimization of novel superjunction LDMOS with partial low K layer

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Abstract: In this paper, a novel superjunction LDMOS with partial low K layer (PLK SJ LDMOS) and linear doping region is presented, which not only breaks the silicon limit, but also overcomes the drawback of SOI devices with lower vertical breakdown voltage (BV). In the x direction, the linear doping optimizes the drift region charge distribution and shields the substrate assisted depletion effect (SAD). Finally, the lateral BV of the device is improved. In the y direction, the LK dielectric in the buried layer strengthens the electric field of buried layer, thereby enhancing the vertical withstand voltage. Simulated results show that the PLK SJ LDMOS with the drift region length of 45 μm can achieve BV of 799 V and figure-of-merit (FOM) of 6.2 MW·cm^{-2}. Compared with the conventional SJ LDMOS (Con. SJ LDMOS), the BV and FOM are improved by 50% and 72.2%, respectively.

Key words: low K; linear doping; substrate assisted depletion effect; breakdown voltage; superjunction.