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Surge protection design with surge-to-digital converter for microelectronic circuits and systems

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ABSTRACT

A surge protection design with surge-to-digital converter is proposed to provide the surge protection for microelectronic products with more flexible applications. The proposed surge-to-digital converter can transfer the occurrences of the surge events into digital output codes by classifying the voltage levels of surge events. It can be used to avoid unwanted power-on reset action, redundant power consumption, or unexpected soft errors, achieving the stability improvement of microelectronic systems. With this surge-to-digital converter, a surge protection design against a surge test of 25 V can clamp the peak voltage of V_{DD} from 22.2 V to 5.6 V. The proposed converter has been verified in a 0.18-μm CMOS process.

1. Introduction

As the CMOS technology scaling down, the reliability issue, such as system-level EOS (electrical overstress) event, plays an important role in the semiconductor industry nowadays. Surge events which have overstressed duration in microseconds can be induced on power lines from power system switching transients or lightning strikes. IEC 61000-4-5 has specified the method of surge immunity test that has been widely applied on microelectronic products [1]. The surge waveforms of 8/20-μs short-circuit current waveform and 1.2/50-μs open-circuit voltage waveform had been defined in the standard. Fig. 1 shows the calibrated 1.2/50-μs voltage waveform which is used in this work. To enhance surge robustness of the microelectronic products, some passive discrete elements (Transient Voltage Suppressor or Gas Discharge Tube) are typically applied to dissipate surge energy [2–4]. However, the excessive heat contributed from residual voltage of surge events can be harmful to the unprotected electrical devices. In previous study, on-chip protection design with big MOSFET clamp has been reported [5]. The voltage detector, transistors, and RC timer are used to detect surge events and then trigger the MOSFET clamp to relieve residual surge energy. However, the MOSFET clamp of a fixed size was often turned on to discharge the surge current without considering the voltage level of a surge event. This may result in an unwanted voltage drop on the power source of V_{DD} to re-trigger the power-on-reset operation or even malfunction when residual surge induced on power lines.

In this work, a new surge protection design with 3-bit surge-to-digital converter is proposed to provide adaptable surge protection for microelectronic products. The function of the proposed 3-bit surge-to-digital converter is verified by HSPICE simulation and silicon test chip. The test chip of the converter fabricated in a 0.18-μm CMOS process has further demonstrated that it can successfully transfer different surge voltage levels into digital output codes. The protection application was validated with on-board test.

2. The proposed surge-to-digital converter

Fig. 2 shows the circuit structure of the proposed 3-bit surge-to-digital converter, which consists of three diode-based surge detection circuits to detect different surge levels. The stacked diode structures with different numbers of stacked diodes are used to detect and distinguish different voltage levels of surge events. In the first stage with an output of V_{OUT1}, the M_{nr1} is used to initialize the voltage levels to 0 V at the nodes V_B and V_{OUT1} by a control signal "RESET" of logic "1" (V_{DD}) before and after the surge events. Under normal circuit/system operations, the diode strings are in off-state with limited leakage current. The voltage at the node V_A is around ~0.4 V, which is decided by the device dimension ratio between the diode string and the diode-connected NMOS (M_{n1}). The M_{P1} is switched off by output voltage of INV_1, which is biased at V_{DD} of 1.8 V. After the reset operation on M_{nr1}, the V_B and the V_{OUT1} will be kept at logic "0" of 0 V.

When surge events are applied on V_{DD}, the overshooting voltage on power lines will turn on the diode string to pull up the voltage level of node V_A. With the operation of inverter (INV_1), M_{P1} is turned on to charge up the node V_B from 0 V to 1.8 V. The C_1 can help to store

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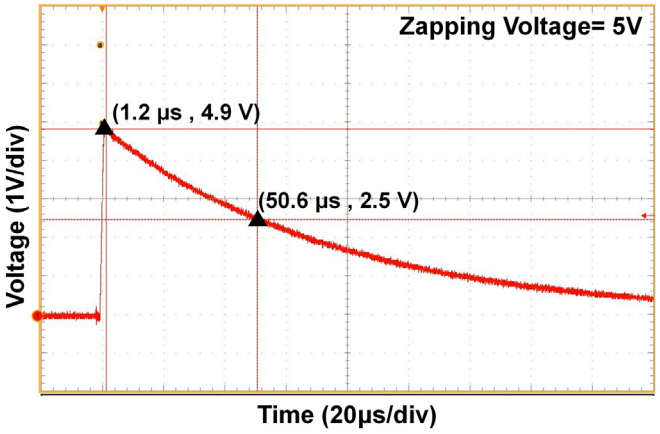

Fig. 1. The calibrated 1.2/50-µs open-circuit voltage waveform of a surge event with a 5-V zapping voltage.

charges at node V_B and in turn to keep the node V_{OUT1} at V_{DD} of 1.8 V. As a result, the V_{OUT1} will transit from logic "0" to logic "1" to memorize the occurrence of a surge event. Similar circuit operation principle is also applied to the 2nd and 3rd stages with the output signals of V_{OUT2} and V_{OUT3}, respectively. The turn-on voltage of the diode string can be linearly adjusted by stacking different numbers of diodes. In addition, the diode-based surge detection circuits can be duplicated and integrated as a multi-bit surge-to-digital converter. Therefore, the converter can distinguish surge voltage levels and transfer them into digital codes after surge events.

3. Simulation results

The detection ability of proposed 3-bit surge-to-digital converter has been simulated by HSPICE. According to IEC 61000-4-5, the surge standard waveform is used in simulations. Fig. 3 presents the simulation results of the proposed converter by applying a 1.2/50-µs surge waveform as surge source. V_{OUT1}, V_{OUT2}, and V_{OUT3} waveforms respond the detection results under different simulated surge levels. The output digital codes of V_{OUT1}, V_{OUT2}, and V_{OUT3} are transited from "0" to "1" sequentially under three simulated surge events with increasing peak voltages, which are shown in Fig. 3(a), (b), and (c), respectively. After the reset signal, all output bits will be reset to "0."

The correlation between the stacked diode number and the surge detection level is presented in Fig. 4. In the test chip, the 3-bit surge-to-digital converter is designed with 2, 3, and 4 stacked diodes to verify its function.

4. Experimental results

The test chip of the proposed 3-bit surge-to-digital converter was fabricated in a 0.18-µm CMOS process with 1.8-V devices. The measurement setup of a surge test is illustrated in Fig. 5. The microphotography of test chip (DUT) is also shown in Fig. 5. According to the standard setting environment of IEC 61000-4-5, a surge tester with 2-Ω effective source impedance and an 18-µF capacitor are used to generate

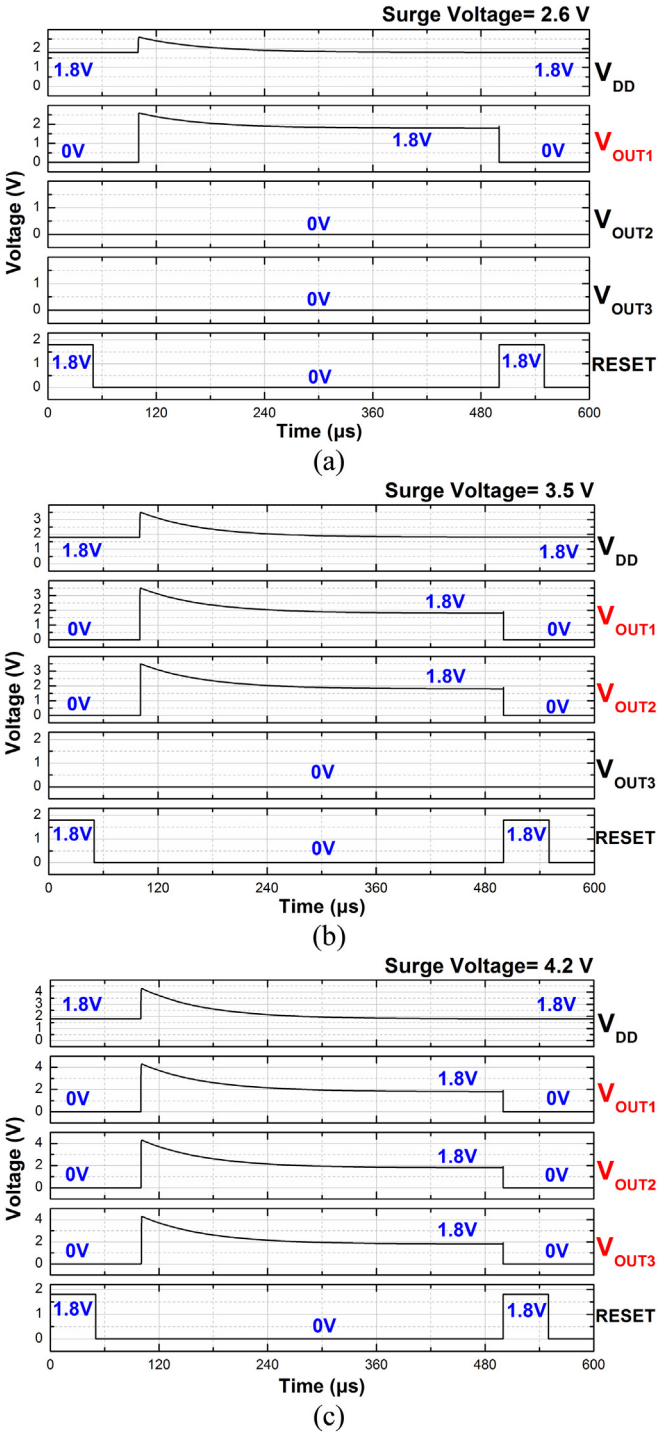

Fig. 3. Simulation results of the proposed 3-bit surge-to-digital converter under surge test voltages of (a) 2.6 V, (b) 3.5 V, and (c) 4.2 V.

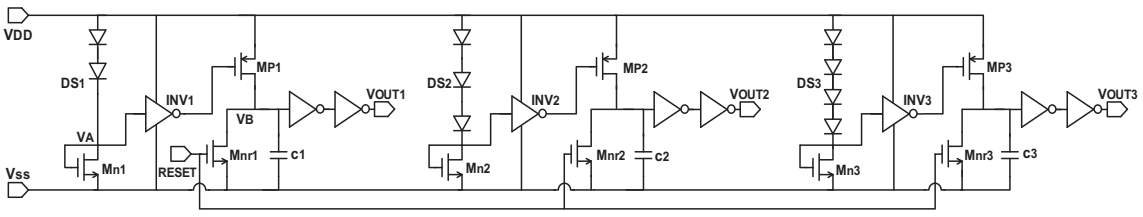

Fig. 2. Circuit implementation of the proposed 3-bit surge-to-digital converter.