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Performance-reliability trade-offs in short range RF power amplifier design

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ABSTRACT

In this work, trade-offs between performance and reliability in CMOS RF power amplifiers at the design stage are studied. The impact of transistor sizing, amplifier class and on-chip matching network design are explored for a 130 nm technology and the implications of design decisions in transistor gate oxide reliability are discussed and projected. A strong trade-off is observed between efficiency and reliability, mainly for different on-chip output matching architectures. A comparison between two example designs is performed via SPICE simulations that include reliability models and the effects of aging on the stress conditions of each amplifier.

1. Introduction

Short range RF Complementary Metal Oxide Semiconductor (CMOS) transmitters are flourishing in the current Internet of Things (IoT) paradigm for a wide range of applications including health monitoring [1]. In this scenario, critical applications involving this kind of circuits require a conscientious evaluation of reliability at a design stage, exploring trade-offs between performance aspects and expected reliability.

Transistor level reliability hazards have been widely studied to ensure a suitable working lifetime for products along the CMOS technology roadmap. Constant downscaling and increasing electric field in transistors made of time dependent dielectric breakdown (TDDB) [2] and Hot Carrier Injection (HCI) [3] a severe threat to device oxide reliability. But a majority of this research has been focused at the product level for, mostly, digital devices with very large scale of integration. Nevertheless, many efforts have been carried on so far to take reliability models into account to predict and implement on-chip strategies for reliability in RF circuits [4–7], but usually centred on analysis or simulation of a given design instead of incorporating the reliability aspect into a design space or architecture exploration.

In this work, we focus on class A-to-C power amplifiers (PAs) working at 2.455 GHz, fully integrated in a 130 nm RF CMOS technology. We propose a design stage exploration of reliability in terms of the matching resistance at the output, taking into account the trade-offs present during matching network design. TDDB and HCI effects are introduced in the design exploration as the two main reliability hazards for PAs. To evaluate the design approach, a simulation study is performed on different PA designs in SPICE, each with a different output matching network topology, and the trade-offs between reliability and circuit performance are discussed. The remainder of the work is organized as follows: Section 4 revisits the TDDB and HCI models and summarizes the approach applied in this work; Section 5 discusses a design exploration of the trade-offs in PA design taking into account reliability indicators; Section 4 shows the comparative results between PA designs based in reliability aware SPICE simulations; finally, Section 5 draws the conclusions.

2. Transistor reliability models

2.1. Time dependent dielectric breakdown

TDDB is a stochastic phenomenon that has been modelled through percolation theory: the applied electric field and the leakage current through the gate oxide contribute to the build-up of defects until a percolation path is created spanning the oxide, forming a conductive path between the channel and the gate contact. The failure rate is characterized by Weibull statistics and strong power law or exponential voltage acceleration of the time to breakdown [2]. In this framework, circuit modelling of the transistor under Soft, Progressive and Hard Breakdown (SBD, PBD and HBD respectively) has been performed through resistors representing the conductivity of the percolation path

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Table 1
Summary of degradation models.[a]

$$t_{63} = \frac{T \cdot t_0}{\left(\frac{A_{ox}}{A_{ref}}\right)^{1/\beta} \int_0^T |V_{G(S/D)}(\tau)|^m d\tau} \quad (1)$$

$$t_{100ppm} = t_{63}(-\ln(1-10^{-4}))^{1/\beta} \quad (2)$$

$$\mu_{HCI} = \frac{\mu_0}{\left(\frac{\Delta V_{thHCI} C_{ox}}{q \alpha_{HCI}} + 1\right)^{m_\mu}} \quad (3)$$

$$\Delta V_{thHCI} = \frac{q}{C_{ox}} K_{HCI} \sqrt{Q_i}\, e^{\frac{E_{ox}}{E_0}} e^{-\frac{\Phi_{it}}{qlE_m}} t^{n_{HCI}} \quad (4)$$

$$E_m = \frac{V_{ds} - V_{dsat}}{l} \quad (5)$$

$$E_{ox} = \frac{V_{gs} - V_{th}}{t_{ox}} \quad (6)$$

$\beta = 1.5$	$m = 11$	$t_0[s] = 6 \times 10^{11}$
$K_{HCI}\,[nm \cdot \sqrt{C}] = 1.7 \times 10^8$		$\alpha_{HCI} = 5$
$E_0[V/nm] = 0.8$	$\lambda[nm] = 7.8$	$n_{HCI} = 0.44$
$l[nm] = 34$	$m_\mu = 1.6$	$\Phi_{it}[eV] = 3.7$

[a] Technology dependent parameters for TDDB models. Values are extracted from the literature: β is the Weibull slope [2], m is the voltage acceleration [2, 10], t_0 is the displacement of the t_{63} vs. VG curve fitted from [2] and references therein. Technology dependent parameters for HCI models. Values are extracted from the literature: K_{HCI} is a fitting parameter [5], α_{HCI} is a proportionality factor that depends on substrate doping [5], E_0 is HCI-driven defects activation energy [5], λ is the mean free path [9], n_{HCI} is the time acceleration factor, l is the pinch-off region approximate length [9], m_μ is the power law acceleration of mobility degradation and Φ_{it} is the minimum energy required to create a defect [9].

[8].

TDDB models characterize time to failure by a Weibull distribution with shape factor β for a technology with a voltage power acceleration factor m, which allows to extrapolate a reference time to failure (100 ppm failed parts in this work, t_{100ppm}). This acceleration factor was chosen to fit the projected lifetime of a 2.2 nm thick SiO2 (as for the technology used in this work) [10]. It should be pointed out that m can take different values at accelerated degradation conditions due to the reduction of defect generation probability at low voltages, as shown by long term (2 years) experimental results [2]. Expressions 1 and 2 in Table 1 show the dependences with voltage and technology of the Weibull characteristic time t_{63} and the extrapolation to lower failure rates t_{100ppm} through the Weibull inverse function.

As per SBD and PBD, numerous models have been developed to represent the conduction through a nanometric percolation path that presents relatively high resistivity (from tens to thousands of kΩ) with a strong dependence on stress time and voltage [11]. However, the high resistivity of a SBD path has been shown to have negligible impact on PA operation [12]. This will be briefly discussed in the next section of this work.

After HBD, the final resistance of the BD path has been shown to range from a few to tens of kΩ with a strong dependence on the relative position of the path in the channel [8]. Under these conditions it is possible to adopt a single β to characterize TDDB for this particular circuit under test. As per the modelling of such breakdown paths in the circuit level, a common approach [6] is to place resistors connected between gate and source (R_{GS}) or gate and drain (R_{GD}) according to the region of the gate where the BD event is considered to take place. Multiple gate oxide breakdown events can be considered in order to accurately predict the degradation of a circuit with time [13], but it will be shown that the impact of such events is strongly dependent with the dominant degradation mechanism for a certain design and can be therefore pondered in a design stage before any simulation models are implemented.

2.2. Hot carrier injection

HCI is a degradation mechanism that has been mainly linked to Si—H bond breaking [3], which is driven by the high electric fields in the channel (mainly in the vicinity of the drain). Channel carriers acquire sufficient energy from these fields to surpass the oxide-semiconductor barrier. The main consequence of energetic carriers in the channel is the injection of charge into the dielectric, causing an overall deviation in threshold voltage (Δv_{thHCI}) and a reduction in the effective mobility (μ_{HCI}). Hence, this effect translates into time dependent parametric degradation of the device that has a strong impact on the RF performance both at the device and at the circuit level [3–7]. As an electric field-driven phenomenon, HCI has been widely characterized to have exponential dependence on drain and gate voltages (V_{DS} and V_{GS}), and to have a power law characteristic with time [9], as shown in Eqs. (3) to (6) in Table 1. Finally, although the effects of RF stress on the impact of TDDB and HCI on device performance has been reported in the literature, there is no general model to assess the impact of the RF stressing conditions on device reliability. It has been proposed in [16] that oxide degradation under RF stress conditions shows a correlation with RMS voltages. On the other hand, the quasistationary sum (QS) of DC signals has shown good agreement with experimental results in [14]. In this work, the latter approach [14] is adopted as it imposes a worst case scenario in terms of the degradation prediction of the circuit under study.

A summary of the models considered during design exploration and circuit simulation is shown in Table 1, along with the adopted values for the technology dependent parameters involved in each model. In these expressions, T stands for the period of the RF signal, t_0 is the displacement parameter of the t_{63} power law acceleration model, A_{ox} and A_{ref} are the device under test and reference areas for area scaling (where half the total Aox is assumed as a rough approximation for GS or GD breakdown). For HCI models, μ_0 is the mobility parameter of a fresh device, Cox the oxide capacitance per unit area, q the electron charge, E_{OX} is the vertical electric field (due to V_{GS}), E_m is the lateral electric field. Model-specific parameters are defined in the footnote of Table 1. It should be pointed out that technological parameters are strongly dependent of technology node and fabrication process, therefore parameter spread can be expected for different manufacturers. In this work, typical parameter values for a 130 nm CMOS node were considered.

3. Design trade-offs for reliability in RF PA

3.1. Impact of BD path modeling on PA performance

Modelling of the BD path between gate and source or gate and drain can show very different sensitivities in terms of circuit performance. This can be explained by the impact of such resistors on the RF performance of the device. While RGD has a direct impact on the transducer gain, RGS impacts introducing an impedance mismatch at the input of the circuit, without any impact on the transducing characteristics. Therefore, same performance degradation of the PA is observed for slightly higher values of RGD than RGS, so RGD can be considered as a worst case from the point of view of its impact on reliability.

In terms of impedance, as the whole circuit operates at relatively low impedance values (tens of Ω), high valued resistive breakdown paths don't represent a hazard for performance of the PA. For the process used in this work, considerable degradation of PA performance is only observed for resistances $< 2K\Omega$. Under this condition, for such low values of RGD and RGS required to observe a clear degradation of circuit performance, it is fairly accurate to only consider severe gate dielectric breakdown (i.e. HBD) in the reliability estimation of a PA.

3.2. Design exploration for reliability

The PA is a circuit block where high voltages and currents are handled, thus pushing reliability limits. RF PA design is most often a trade-off between linearity, area consumption and power efficiency at a