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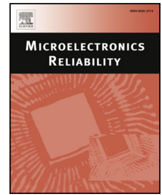

Smart SiC MOSFET accelerated lifetime testing

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ABSTRACT

Accelerated lifetime testing of power modules is time consuming and expensive due to the destructive nature of these tests. Therefore, it makes sense to extract as much data as possible from each consumed component. Traditional power cycling methods, however, monitor a single parameter and stop the test after this parameter reaches a predefined threshold. This leaves little data available for real-time analysis of the aging process, which instead must take place post-failure. In this paper, we present full results from a power cycling test on SiC MOSFETs which uses a novel method to extract both the semiconductor die resistance and bondwire resistance separately. Using this method, we are able to observe degradation phenomena that has previously been hidden when using conventional monitoring methods. We hope that the presentation of this data will demonstrate the incentive to incorporate smart monitoring functions during accelerated lifetime testing of power semiconductors. In essence, we aspire to advance the techniques in this area to provide a 'window' into the module, which allows the failure process to be accurately observed in real time. In turn, we hope these methods will allow more targeted improvements to module design from a reliability perspective.

1. Introduction

1.1. Accelerated lifetime testing in power modules

Power semiconductors are among the most expensive and unreliable components in power electronic systems. They are used to provide high efficiency power conversion in applications encompassing renewable energy generation, automotive, railway, aerospace and motor drives. Reliability is of utmost importance for both economic and safety reasons. Therefore, power semiconductor module manufacturers and their customers spend considerable resources on assessing the reliability aspects of these components.

Reliability assessment of power semiconductor modules is commonly performed using accelerated aging test procedures known as power cycling. The modules are mounted on a heatsink and a forward current is applied. This current through the device leads to a power loss throughout the entire module and results in an increase in semiconductor junction temperature. By periodically switching the current on and off, the temperature of the semiconductor will rise and fall accordingly. This temperature swing induces thermomechanical stress which ages the module. One period of heating and cooling via the conducting current is generally referred to as a 'power cycle'. Depending on the absolute temperature swing, module type, and test procedure, it may take anywhere between a few thousand, to tens of millions, of power cycles until module fails [1].

Fig. 1 displays a depiction of the above described traditional power cycling test on a power semiconductor module. Power cycling tests are generally time consuming – commonly used cycle periods are between 0.2 s to 1 min [1] – so testing with high numbers of power cycles can take up to several months [1,2].

In most power cycling tests, an electrical parameter is monitored and the test is stopped after this parameter reaches a predefined threshold indicating that the device is at the end of its life.

The most commonly used failure parameters are the collector-emitter voltage (V_{CE}) and thermal resistance (R_{TH}) [1,3,4]. According to a 2016 survey on power cycling tests [1], over 60% of power cycling tests select an increase of between 5 and 20% in V_{CE} or R_{TH} as the indicator to conclude the test, while 8% of studies simply wait until the module reaches complete failure. The monitored failure parameter may often be recorded with little resolution and primarily used as a trigger to signal the conclusion of the test.

This approach is adequate if the goal of the power cycling test is to validate that a module can survive a certain number of power cycles, or acquire data for the generation lifetime models.

However, basic monitoring such as the above provides little data to examine for insight into the degradation process as the test progresses, i.e. the degradation process cannot be observed in real-time, and the final cause of failure must be determined using post-failure analysis.

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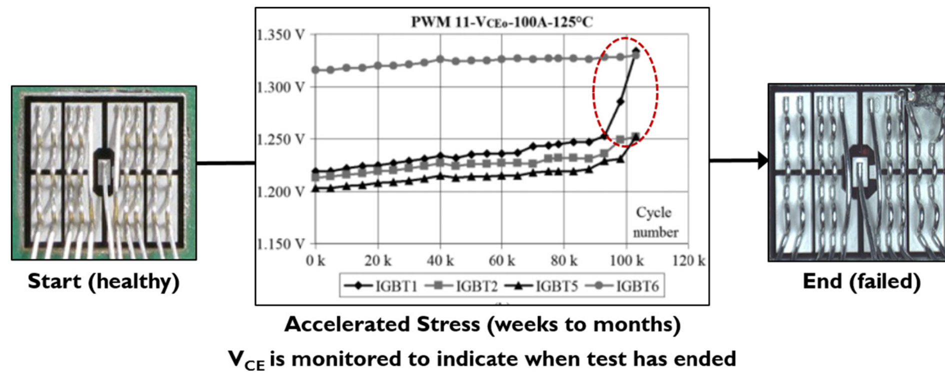

Fig. 1. Graphical depiction of a power cycling test on IGBTs, all figures taken from [5].

Since up to 40% of power cycling tests are performed with the intention to analyse the failure process (along with the influence of design changes on this process) [1], it would make sense to have data regarding the entire aging process, rather than a 'before and after' picture as is common now. This would also provide efficient use of the time consumed in power cycling tests with large amount of power cycles to complete.

1.2. Silicon carbide MOSFETs

Silicon Carbide (SiC) MOSFET modules are often cited as a future alternative to Silicon (Si) IGBTs that will allow operation of power converters at higher frequency, efficiency, and temperature. They are now commercially available with current ratings of several hundred Amps. Nevertheless, the reliability, and reliability testing procedures for SiC MOSFET modules remain an important issue.

First of all, SiC has different material properties in comparison to Si. The coefficient-of-thermal-expansion is slightly higher in SiC, while the Young's Modulus is 3 times higher. The result of this is differing thermo-mechanical strain inside the semiconductor for SiC and Si chips of identical geometry. Early power cycling results on SiC devices have shown a reduced power cycling capability in comparison to Si devices, when transferring standard packaging techniques across to the SiC device [6].

Secondly, the failure mechanisms for SiC MOSFETs can be different to those of Silicon IGBTs. Therefore, the typical degradation indicators such as the V_{CE} (on-resistance in MOSFETs) or R_{TH} are unlikely to behave in the same manner. A prominent example of this is the instability of the threshold voltage in SiC MOSFETs, which can alter the measurement of both of these parameters [7,8].

This can be seen in early publications regarding SiC MOSFET power cycling tests [8,9]. For example, Fig. 2 shows the evolution of the on-resistance (R_{ON}) of a SiC MOSFET during an accelerated aging test from 2013 [9]. The R_{ON} increases over 60% from the original value without the device experiencing a failure. It is not possible to ascertain what mechanism is causing this increase (i.e. whether it is packaging related or semiconductor die related), nor whether the device is actually close to failure, unless post-failure analysis is used.

A further issue is that the cost per component for SiC MOSFETs is an order of magnitude greater than Si devices. Therefore, it makes sense for reliability researchers to be able to maximise the amount of data collected from each SiC MOSFET during power cycling tests, in order to understand more quickly the degradation process without incurring unnecessary financial expense.

1.3. Paper objectives

Power cycling on Si IGBTs is very well established, with over 60% of all studies being performed on the IGBT from 1994 to 2016 [1]. Nevertheless, the issues outlined above regarding SiC MOSFETs having

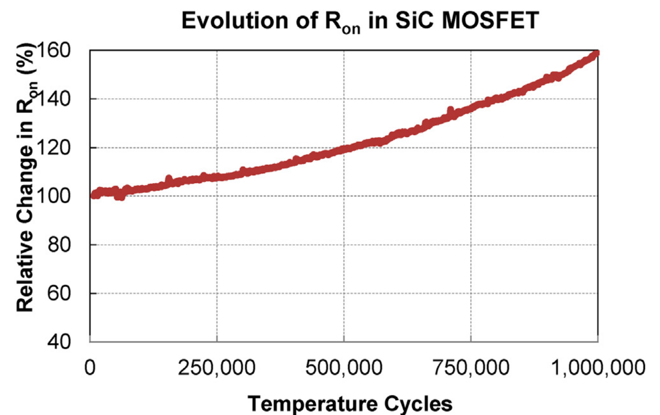

Fig. 2. Evolution of R_{ON} of a SiC MOSFET in TO-247 packaging during a power cycling test [6].

differing material properties, failure mechanisms, and the high cost per component, mean that we feel that directly transferring power cycling techniques from Si IGBTs to SiC MOSFETs is not an efficient strategy.

In particular, we feel that there is the need (and opportunity) to increase the amount of acquired data during the power cycling process. Monitoring a single failure parameter to trigger the conclusion of the power cycling test is inefficient in both time and money in order to gain insight into the aging process inside the SiC MOSFET.

As a result, in his paper we will present full results from a power cycling test on SiC MOSFETs which uses a novel method to extract both the semiconductor die resistance and bondwire resistance separately. We monitor both parameters with high measurement and temporal resolution, which enables monitoring of the bondwire resistance to μΩ resolution.

Using this method, we are able to observe degradation phenomena that has previously been hidden when using conventional monitoring methods. We would like to note that the presented monitoring method can also be used in Si IGBTs, however the spur to develop this method was brought upon by the issues with SIC MOSFETs highlighted in Section 1.2.

2. Power cycling test bench

2.1. Semiconductor die and bondwire resistance monitoring

The origins of the test bench stem from the use of the auxiliary-source terminal which is common in many SiC MOSFETs (although not all) due to their fast switching nature. The auxiliary-source terminal is present in SiC MOSFETs to provide the reference potential for the gate control voltage. This separates the current path of the control current from the path of the load current, and results in increased switching

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