Microelectronics Reliability 88–90 (2018) 122–127

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

A body built-in cell for detecting transient faults and dynamically biasing subcircuits of integrated systems

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ARTICLE INFO

Keywords:
Body biasing
Transient fault detection
Level-shifter
BBICS

ABSTRACT

Power consumption and reliability are nowadays the main concerns for nanoelectronic systems. In fact, these factors are closely related, the reliable operation of a system is strongly associated with its power supply voltage (V_{dd}), frequency of operation, and body biasing. Therefore, power management and fault tolerance techniques need to be jointly implemented to guarantee better overall low-consuming and reliable solutions. This paper presents a novel body built-in cell to address these two issues. It is capable of: 1) detecting short-duration and long-duration transient faults (TF), thus enhancing system's reliability; 2) controlling the circuit's threshold voltage (V_{th}) through the implementation of adaptive body biasing (ABB) schemes, thus optimizing the system's trade-off between low-power and high performance.

1. Introduction

Power consumption and reliability are nowadays one of the main concerns for nanoelectronic systems. Although in the past the dynamic energy has been the dominant source of consumption, in the deep submicron era the significantly increased sub-threshold leakage is making the static power comparable to the dynamic consumption [1]. Therefore, guaranteeing low-power operation in advanced technology nodes require the use of techniques to mitigate leakage. In this context, adaptive body bias (ABB) has been shown to be an effective alternative to overcome this issue [2,3]. By artificially increasing transistors threshold voltage (V_{th}), the leakage is reduced, a scheme known as reverse body biasing (RBB). Alternatively, decreasing V_{th}, a technique known as forward body biasing (FBB) increases transistors performance. Implementing such schemes requires special cells that need to be embedded to the system, properly controlling the body bias voltage (V_{BB}), commonly known as body bias generators (BBG) [4,5]. Implementations based on level-shifters represent a promising solution, specially for fine-grain biasing, due to their simplicity and low area overhead [4].

Another major challenge faced by nanoelectronic systems is reliable operation, specially for applications in which failure is critical, e.g. satellites, aircrafts, and nuclear power plant robots. The harsh environment in which such devices are inserted are susceptible to high radiation exposure or environmental variations, that may induce parasitic transient currents.

These faults (TF), which are indeed temporary voltage level modifications, affect the circuits for a short duration of time, and their occurrence are not predictable. Consequently, TFs need to be detected and corrected at run-time to avoid the occurrence of soft errors. Among the existing design strategies for detecting TFs, the Body Built-In Current Sensors (BBICS) [6,7] offer a promising solution that is perfectly suitable for system design flows based on CMOS standard cells [8].

In fact, the robustness of a system is strongly related to its frequency of operation, the power supply voltage (V_{dd}), and V_{BB} [9]. Thus, power management and fault tolerance techniques need to be jointly considered. Studies have shown that FBB reduces the soft error rate induced by radiation, while applying RBB increases it [10,11]. Furthermore, both ABB and transient fault detection techniques require special cells to provide the appropriate V_{BB} for transistors.

This paper presents a novel cell that merges the functionalities of BBICS and level-shifters based BBGs. Therefore, the proposed architecture is capable of: 1) detecting short-duration, or long-duration TFs; 2) controlling V_{th} thus compensating alterations induced by aging or PVT variations; 3) optimizing the system's trade-off between low-power and high performance. The design of a single cell with multiple purposes allows to further reduce the already low area overhead imposed by the elements of the BBICS and level-shifter circuitry. It also facilitates the cell insertion to a standard design flow.

The following sections of this work are organized as follows:

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https://doi.org/10.1016/j.microrel.2018.07.069
Received 31 May 2018; Received in revised form 2 July 2018; Accepted 5 July 2018

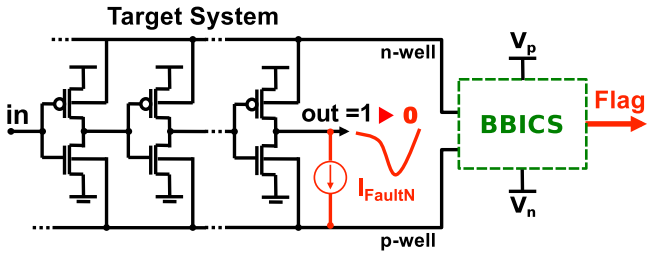

Fig. 1. Abstraction of BBICS monitoring a generic target system. The red current source models the occurrence of a transient fault. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

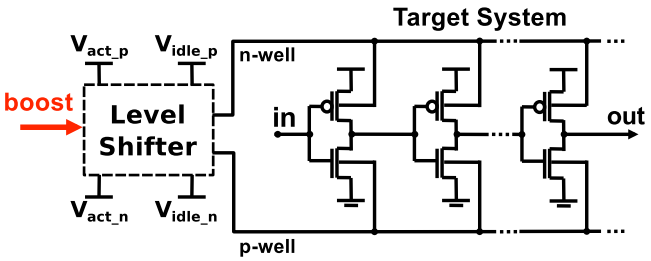

Fig. 2. Abstraction of a level-shifter based BBG controlling the V_{th} tuning of a generic target system.

Section 2 presents the fundamental on detecting TFs with BBICS and how to implement ABB schemes. The following section describe the architecture and the behavior of the proposed body built-in cell, and precises how it is used for both body biasing and TF detection. Section 4 explains the experiments conducted and the results obtained with the proposed architecture inserted into a target circuit, and Section 5 concludes this work.

2. Fundamentals

2.1. Detecting TFs with BBICS

The so-called body or bulk built-in current sensors (BBICS) are used to detect abnormal transient currents flowing from the body to the drain (or vice versa) of sensitive transistors (reverse-biased PN junctions) of a design under test (DUT) [6]. Fig. 1 depicts an abstraction of a BBICS monitoring a target system. It shows a current source (I_{FaultN}), that models a transient fault (TF) occurring in one of the NMOS transistors of the target system. As shown in Fig. 1, the voltages that bias the body of the NMOS and PMOS transistors (V_n and V_p respectively) are provided by the BBICS. Thus, there is no direct connection between the body terminals of the target system and the power rails, as depicted in Fig. 1. Whenever an atypical current is detected, an output flag is raised (Flag signal in Fig. 1), indicating the occurrence of a TF. The threshold at which the BBICS is capable of detecting a TF is defined as the BBICS sensitivity and it is determined by the number of transistors in the target system and the architecture of the BBICS [12]. Therefore, two strategies are used to calibrate the range of TF detectable by a BBICS: 1) splitting the target system into sub-circuits, each one of them monitored by an independent BBICS, thus reducing the number of monitored transistors per sensor; 2) changing the size and drive strength of some specific transistors of the BBICS. In this work, for the sake of simplicity, only the NMOS sensor is analyzed. The analyses of the PMOS case are analogous.

2.2. Implementing ABB schemes

Applying a biasing voltage to the n-well and p-well of transistors changes their V_{th}, a technique known as body biasing. If V_{th} is increased, through a RBB scheme, the leakage is reduced and so does the performance. Alternatively, decreasing V_{th} allow improving transistors performance at the price of higher leakage consumption, a technique known as FBB. The attractiveness of RBB and FBB is increased by implementing an adaptive body biasing (ABB) scheme. The idea is to decrease V_{th} during active periods, to enhance circuit's performance, and increase it during idle periods to prevent unnecessary leakage. Implementing such ABB schemes requires special cells, known as body bias generators (BBGs), capable of changing the biasing voltage of the n-well and p-well during circuit operation. The scientific literature on BBGs is very dense, with several propositions of architectures for addressing different applications [5,13-16]. Many of the proposed designs use DACs and/or charge pumps to generate V_{BB} with a fine resolution [5,13-15]. Although this is a good solution for charging large systems, BBG's complexity and high area overhead make them inappropriate for biasing small parts of systems. This work is focused on applying ABB in sub-circuits of an integrated system, therefore, the complexity and area overhead of BBGs need to be minimized. A strategy based on V_{th} hopping [4,16] is used for that purpose. The idea is to reduce the resolution of V_{BB} by setting only two possibilities: one voltage level for decreasing V_{th} and another one for increasing it, which is easy implemented with level shifters.

Fig. 2 depicts an abstraction of the ABB strategy used in this work. The level shifter block controls the tuning of the transistors V_{th} depending on the target system's activity. Whenever the boost signal is 1, indicating that the target system is active, the body of the transistors will be set to V_{act_n} and V_{act_p}, voltage levels that decrease V_{th}, thus increasing the performance. Conversely, if the boost signal is 0, which indicates that the target system is idle, the body of transistors are biased to V_{idle_n} and V_{idle_p}, a configuration that increases V_{th}, consequently decreasing the leakage.

The body biasing strategy shown in Fig. 2 applies to both RBB and FBB schemes. In fact, what differentiates these strategies is the choice of voltage levels of V_{idle_n}, V_{idle_p}, V_{act_n} and V_{act_p}. For instance, in order to implement FBB $V_{idle\_n} = 0$; $V_{idle\_p} = 0$; $V_{act\_n} > 0$; and $V_{act\_p} < 0$. $V_{act\_p} < 0$. The experiments described in Section 4 were performed with FBB. The procedure to perform simulations with a RBB scheme is analogous to what is described in Section 4.

The feasibility of level-shifter based BBGs for ABB relies on: 1) low delay, rapidly switching from low-leakage to high-performance mode and vice versa; 2) very low power consumption, in order to minimize the power overhead; 3) proper operation at low V_{dd}, in which minimum energy is reachable [17]. Therefore, these parameters are used in the experiments described in Section 4 to evaluate the efficiency of the proposed body built-in cell for implementing ABB schemes.

3. Proposed body built-in architecture

The body built-in cell proposed in this work unites the strategies described in Sections 2.1 and 2.2. Therefore, the proposed architecture is composed of two parts: a level-shifter based structure, depicted in Fig. 3 inside a dashed black box; and a current sensor based structure, shown inside the dashed green box of Fig. 3. The body built-in cell described in this paper corresponds to the circuitry necessary for biasing and monitoring the NMOS transistors of a target system. The architecture for the PMOS network is analogous.

3.1. Level-shifter structure

This part of the proposed body built-in cell ensures a proper implementation of the ABB strategy described in Section 2.2. The functionality of the level shifter of Fig. 2 is implemented by the circuitry inside the dashed black box of Fig. 3. Therefore, if the input signal boost