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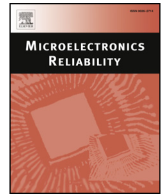
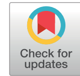


Towards understanding recovery of hot-carrier induced degradation



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ABSTRACT

This article treats the recovery of hot-carrier degraded nMOSFETs by annealing in a nitrogen ambient. The recovery rate is investigated as a function of the annealing temperature, where the recovery for increasing temperatures is in agreement with the passivation processes. At the original post-metal anneal temperature of $T = 400$ °C, the device's original performance is fully restored. Higher temperatures induce a permanent, unrecoverable change to the devices, manifested in a gradual V_T shift. The recovery rate is found to be independent of both the transistor gate length and the cooling rate (quench, slow and stepped cooling) upon annealing. These findings are used to gain further understanding of the mechanisms behind the recovery of hot-carrier damage. The recovery rate exhibits Arrhenius behavior and the recovery data are consistent with Stesmans' recovery model.

1. Introduction

Several degradation mechanisms like hot-carrier injection (HCI) and bias temperature instability (BTI) arise when an electrical stress is applied to nMOSFET's. Charge trapping, defect formation in the gate oxide and at the interface play a role, although there is still some discussion to what degree [1]. There is however consensus that for both mechanisms hydrogen plays a pivotal role in the degradation and recovery of the devices [2]. Hydrogen may be released from Si-atoms at the interface and the so called P_b-centers, Si-atoms at the interface with a dangling bond, may be created. The defects can act as a charge trap, which can result in a shift of the threshold voltage, ΔV_T.

Less is known about the recovery, however it is assumed that during recovery, hydrogen atoms in the vicinity of the interface may repassivate the P_b-centers [2]. The hydrogen density at the interface is related to the concentration and diffusion of hydrogen species (H, H^+, H_2) in the gate stack. The diffusion rate in Si and SiO_2 is known to be different [3], suggesting that the materials in the immediate vicinity of the defective interface matter for recovery. Furthermore, both bias [4] and temperature [5] affect the recovery rate of the devices.

It is reported that the gettering of hydrogen atoms at grain boundaries in poly-Si films depends on the cooling rate and not on the anneal time itself [6]. A slower cooling rate will getter hydrogen from a bigger area due to a longer diffusion length. This raises the question if the repassivation rate and thus ΔV_T can be affected by varying the gate length of the devices and the cooling rate, schematically visualized in Fig. 1.

The motivation behind this work lies in the pursuit of self-healing transistors, see *e.g.* [7] and [8]. To investigate the properties of the recovery mechanism, the spontaneous recovery in a nitrogen ambient is investigated as a function of the temperature, the gate length and cooling rate. It is expected that V_T and the subthreshold swing will decrease and g_m, $I_{d,lin}$ will increase during recovery.

2. Experimental

2.1. Temperature dependence

The devices under study were long-channel nMOSFETs with a gate width of $W = 10.0$ µm, a gate length varying between $L = 0.6$ µm and $L = 10.0$ µm and a gate oxide thickness of $t_{ox} = 4.5$ nm. Annealing was done die for die, where each die contained nMOSFETs of all the gate lengths. Since the slow, long-term degradation and recovery of HCD were investigated, measurements were done using the measure-stress-measure (MSM) method. The threshold voltage of the pre-stress measurement is used as reference for maximum passivation and a reference for further measurements. Measurements were performed with a Keithley 4200-SCS and four Keithley 4200-PA Remote PreAmps for the source, drain, gate and bulk contacts. For the V_T-extraction, the drain bias was kept at $V_{ds} = 0.1$ V and the gate voltage was swept from $V_{gs} = -1$ V to $V_{gs} = 3$ V in steps of 25 mV at $T = 25$ °C. Using the extrapolation in the linear region (ELR) of the maximum transconductance, $g_{m,max}$, V_T was extracted [9]. The subthreshold swing, *SS*, is determined between $V_{gs} = 0.05$ V and $V_{gs} = 0.4$ V, $I_{d,lin}$ is determined

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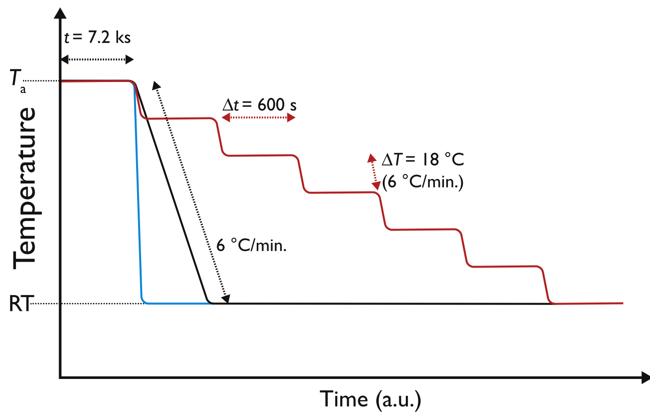

Fig. 1. Different types of cooling process, quench cooling (blue), slow cooling (black) and stepped cooling (red) from the annealing temperature (T_a) to room temperature (RT). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

at $V_{gs} = 2$ V.

During electrical stress, a constant voltage stress (CVS) was applied to the device at a temperature of $T = 25$ °C for a cumulative time of 3 ks if not otherwise specified, where two electrical measurements were performed per decade of stress time. The applied source-drain bias was kept at $V_{ds} = 4.5$ V and the source-gate bias was kept so that $|I_b|$ was maximum, which varied between $V_{gs} = 1.75$ V to $V_{gs} = 2.1$ V for the devices with a gate length of $L = 0.6$ μm to $L = 1.0$ μm. A source-drain bias of $V_{ds} = 6.5$ V and a source-gate bias of $V_{gs} = 1.7$ V was applied to the devices with a gate length of $L = 10.0$ μm. There was a delay of 1 s between the stress and measurement phase, to minimize short time-scale recovery components. The results are from one device and to minimize the variance, 15 measurements were done on the same device to determine the threshold voltage.

Positive bias temperature instability (PBTI) was measured on separate devices under identical conditions as for HCI, but with source and drain kept at ground. The threshold voltage was measured after 1 s delay, to investigate the long-term BTI contribution to ΔV_T under the HCI condition. No significant shift in the threshold voltage was measured after BTI stressing, indicating that it can be neglected for the devices that underwent HCI.

After electrical stress, the devices were annealed die for die in a nitrogen ambient (ramp rate: ~8 °C/min) according to Fig. 2 for 60 min. The bias on contacts of the device were kept floating during the anneal. After electrical measurements, the devices were annealed again in a nitrogen ambient for increasing higher temperatures (between $T = 100$ °C and $T = 540$ °C). After the anneal at $T = 500$ °C, an anneal at $T = 400$ °C and an anneal at $T = 350$ °C were done again, each followed by electrical measurements.

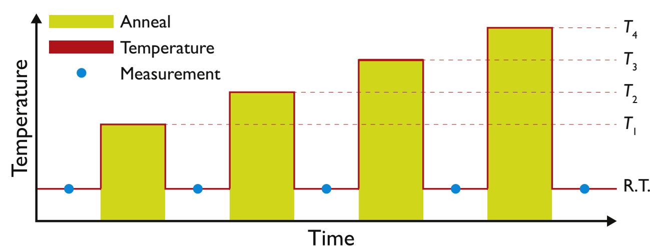

Fig. 2. The measurement process to investigate different anneal cycles of a single die. The blue dots represent the moment of the measurement, green represent the moments that the device is annealed and the corresponding temperature is given in red. Four anneal temperatures are given by T_1 to T_4. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

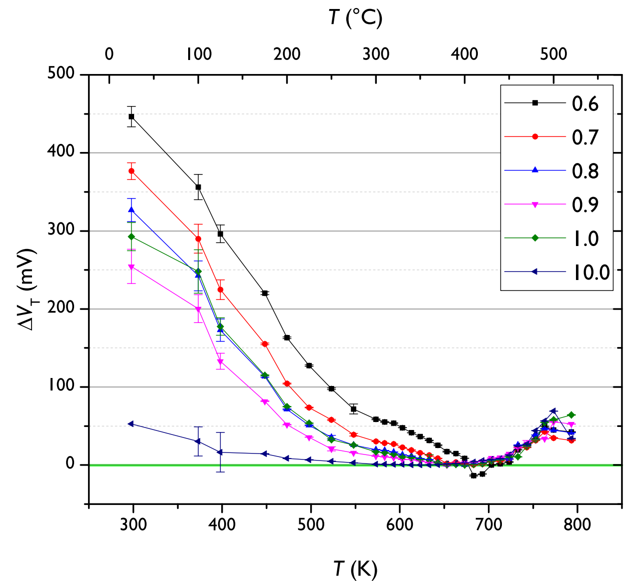

Fig. 3. The shift in the threshold voltage as a function of the applied thermal treatment. The devices have a width of $W = 10$ μm and the legend indicates L in μm. The electrical measurements were done at $T = 25$ °C.

The cooling rate dependency was investigated by stressing the devices for 3 ks. The quench cooling (the blue curve in Fig. 1) was done by removing the device from the furnace. The slow cooling (the black curve) had a cooling rate of 6 °C/min. The stepped cooling (the red curve) was done with steps of $\Delta T = 18$ °C, after which the temperature was kept constant for 10 min. This was done step by step to a temperature of $T \approx 110$ °C, where any extra recovery should be negligible [5].

3. Results and discussion

3.1. Anneal temperature dependence

Fig. 3 shows the recovery as a function of the applied temperature for devices exposed to electrical stress for 3 ks. As expected, a smaller gate length results in more degradation and thus a larger ΔV_T.

There is more recovery after annealing at a higher temperature. After an anneal at $T = 350$ °C to $T = 400$ °C, $\Delta V_T \approx 0$. This temperature coincides with the applied temperature during the post-metal anneal step and corresponds with the various values for total recovery reported by literature [5,10]. The data suggests that the device is completely recovered from the HCD. The devices with more degradation show a higher absolute recovery rate, although normalized to the maximum ΔV_T of each gate length, all devices show similar recovery.

After exposure to higher temperatures, $T > 450$ °C, V_T starts to increase. A temperature of $T \approx 400$ °C corresponds to a thermal energy higher than the bonding energy of Si—H bonds. This temperature range coincides with earlier reported values [6,11], suggesting that more P_b-centers at the Si/SiO_2-interface are introduced by the anneal. The ΔV_T is similar for all devices, suggesting that defects are introduced at the same rate/concentration, regardless of the gate length.

Due to thermal degradation, $\Delta V_T(500\ °C) > 0$ mV. It was checked if the devices could be repaired with an additional anneal at $T = 400$ °C and $T = 350$ °C in an nitrogen ambient (the temperature where total recovery took place). However, no significant shift in V_T was observed after the second anneal at the temperature where total recovery should take place, however these anneals show negligible effect on ΔV_T. After HCD, sufficient hydrogen atoms were present to accommodate re-passivation of P_b-centers. It is reported for some time that at higher temperatures, out diffusion of hydrogen into vacuum can take

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