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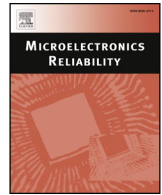

Quantitative correlation between Flash and equivalent transistor for endurance electrical parameters extraction

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ABSTRACT

Nowadays, the study of physical mechanisms that occur during Flash memory cell life is mandatory when reaching the 40 nm and beyond nodes in terms of reliability. In this paper we carry out a complete experimental method to extract the floating gate potential evolution during the cell aging. The dynamic current consumption during a Channel Hot Electron operation for a NOR Flash is a proper quantitative marker of the cell degradation. Here both drain and bulk currents are measured and monitored throughout the endurance tests. We coupled these characteristics with quasi-static measurements to correlate the cell degradation with an equivalent transistor. The final goal is to be able to split the physical effects of repetitive hot carrier and Fowler-Nordheim operations, typical of Flash memories, to extract the electrical parameters evolution on a simple equivalent transistor.

1. Introduction

In the semiconductor non-volatile memories world, we observe an increasing production of resistive switching devices [1–4], even if the floating gate Flash still share a large percentage of the market. The charge storage devices, for embedded applications, are today scaled toward the 40 nm node and beyond [5–7]. The Flash programming scheme has been adapted to satisfy the new constraints imposed by the smart connected object application field, to remain competitive with respect to the new devices, very aggressive in terms of energy consumption and scaling [8, 9]. Last but not least, the cell architecture has been modified in a 2 T memory and split gate (1.5 T) [10–12] or even, using a FD-SOI technology [13]. This kind of improvements can decrease the cell energy consumption and leakages, in order to address the ultra-low power applications. One of the main issues in these new architectures is the coupling factor estimation to evaluate the Flash programming efficiency [14–17]. It is very complicated today to compute the effect of parasitic capacitances once the single cell is arranged in an array. In this paper we propose to adapt the experimental technique presented in [18] to the standard Flash processed by STMicroelectronics. In the first part we describe the measurement setup used for the electrical characterizations and endurance tests on the standard cell and its equivalent transistor. Thus, we show the importance to consider the dynamic source current during a Channel Hot Electron (CHE) operation, to find the real cell coupling factor. In this way it is possible to extract the real floating gate potential (V_{FG}) variation during the programming time (t_P), as qualitatively proposed in [19]. Moreover, in the second section, a smart test algorithm is presented to induce a quantitative degradation on the equivalent transistor corresponding to the memory cell during cycling. The dynamic current consumption will be used as a marker of tunnel oxide degradation for both devices. Thanks to the four fully arbitrary pulse generators, the floating gate potential will be adjusted during cycling. Hence, the drain and bulk current contributions are needed to understand the charge trapping localization. This technique can be useful to characterize equivalent transistor during the parametric test phase, after wafer fabrication to quickly get the cell degradation information. In fact, the future aim is to correlate these results, that has a duration of several minutes, with DC stress measurements and find a way to get the outcome in a shorter time. Moreover, it will be possible to characterize the tunnel oxide using other techniques like charge pumping to make sure that the corresponding oxide degradation is applied. Finally, we will demonstrate the validity of our method, and we show the dynamic characteristics degradation not only in terms of source current but also as a contribution of bulk current that represents here 15% of the global consumption and cannot be neglected. We compare the results of adaptive cycling with the non-adaptive experiment to validate our methodology. The aim is to improve the understanding of tunnel oxide

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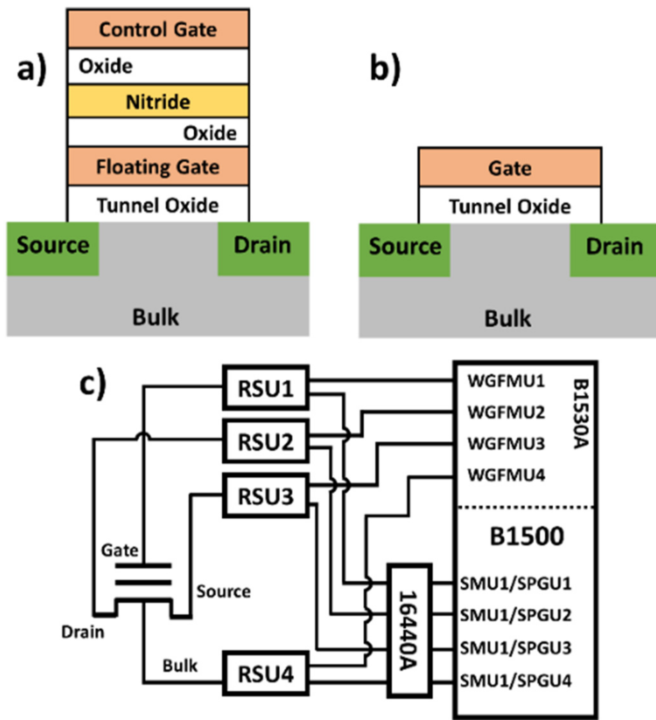

Fig. 1. Block diagram of a) memory cell and b) equivalent transistor. c) Measurement setup.

degradation. This method will enable the evaluation of real cell degradation on an equivalent transistor for quantitative parameters analysis which cannot be directly performed on the memory cell.

2. Experimental details

2.1. Samples and measurement setup

In this work the samples are taken from standard single Flash floating gate memory cells and the related equivalent transistors (dummy cells) are implemented on 200 mm wafers. The cell dimensions are 0.07 µm in width and 0.16 µm in length. The tunnel oxide is a standard thermally grown SiO_2 while the interpoly-dielectric is an Oxide/Nitride/Oxide (ONO) tri-layer stack (Fig. 1a). The equivalent transistor has the same size, with the possibility to directly bias the floating gate (Fig. 1b). A complete set of electrical characterizations have been carried out during the endurance test using the experimental setup shown in Fig. 1c. The block diagram represents the Keysight B1500 equipped with 4 WGFMUs (Waveform Generator Fast Measurement Unit, Keysight B1530A), 4 SPGUs (Semiconductor Pulse Generator Unit) and 4 SMUs (Source Monitor Unit). The switching between SMUs and SPGUs made with the 16440A selector, limiting parasitic elements. We connected in series the RSU (Remote-sense and Switch Unit) modules that enable the link with the probes and the DUT (Device Under Test). In the case of dynamic current measurements, they switch to WGFMU position enabling the fast pulse generation. In this last case the connection between the B1530 and the DUT is fully adapted to reduce the parasitic effect due to the connections. With this method we were able to perform quasi-static (DC) and dynamic measurements to obtain threshold voltage kinetics, pulsed current/voltage characteristics and current consumption plots.

2.2. Coupling factor extraction methodology

The coupling factor (α_G) is the main parameter needed to apply a stress on dummy cell oxide equivalent to the stress of memory cell through cycling. Indeed, it is well known how to compute the floating gate potential as a function of the control gate voltage (V_{CG}) during programming operation [17]. Nevertheless, the calculation of α_G can be complicated because of parasitic capacitances due to the cell environment. Several techniques are available and explained in literature [14–17], but they combine quasi-static measurements on memory and

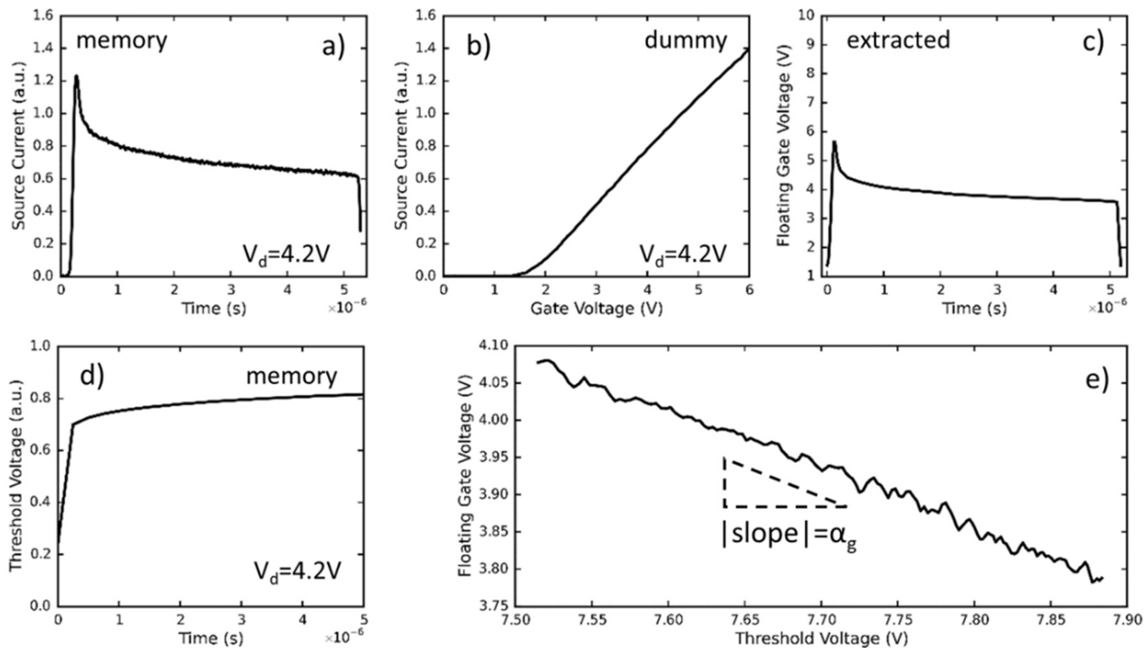

Fig. 2. a) Measured source current consumption of memory cell. b) Measured source current versus fast ramped gate voltage of dummy cell. c) Extracted floating gate voltage during the programming operation. d) Measured memory programming threshold voltage kinetic. e) Floating gate voltage versus threshold voltage characteristic used for the coupling factor (α_G) extraction.

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