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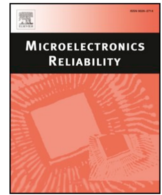
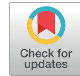


Statistical nature of hard breakdown recovery in high-κ dielectric stacks studied using ramped voltage stress



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ABSTRACT

In replacing the conventional SiO_2 gate dielectric with high-κ materials, new challenges emerge on understanding the kinetics of dielectric breakdown due to the different properties of the new bulk oxide and the interfacial layers at the substrate and gate electrode interface as well. Among several complexities, dielectric relaxation and recovery have received a lot of attention due to their promising applications in resistive random access memory (RRAM). In this study, we explore the *stochastic nature of hard breakdown recovery* in HfO_2, taking advantage of ramped voltage stress (RVS) measurements, which are theoretically equivalent to the widely used constant voltage stress (CVS), while being significantly less time-consuming. We found that the possibility of recovery is largely dependent on the ramp rate during RVS as the dielectric needs adequate time and sufficient thermal budget to recover. The clustering model is found to be a good fit to the RVS data sets for post-recovery subsequent breakdown events and the extent of defect clustering is found to be more intense after increasing number of recovery events. The breakdown mechanism in the stack is confirmed by measuring the resistance change trends with temperature.

1. Introduction

Gate dielectric breakdown (BD) is one of the key concerns on front-end reliability analysis of logic and non-volatile memory devices [1]. The application of high-κ dielectrics in recent years, such as HfO_2, Al_2O_3, La_2O_3 and Ta_2O_5 as a replacement for conventional SiO_2, together with scaling issues has complicated the kinetics of breakdown in sub-32 nm CMOS technology nodes [2,3]. Extensive studies have been carried out to study dielectric breakdown in high-κ stacks using the framework of the percolation model [4–8]. In most cases, the statistical analysis is confined to the soft breakdown and progressive breakdown stages that are more relevant to the operating conditions of the planar and FinFET devices in the field. Recovery of dielectric breakdown has also been reported in soft and hard breakdown scenarios earlier and these recovery phenomena have been attributed to the role of oxygen ion – vacancy recombination as well as metallic filament rupture respectively [9,10]. There is however no detailed investigation into the stochastic nature of the recovery phenomena to date. This includes analysis of the magnitude of recovery, the number of recovery events after the first breakdown, distribution of breakdown voltages for multiple recovery events and any perceived correlation in the extent of breakdown recovery and its impact on the next breakdown voltage during a ramped voltage sweep. In this study, we hope to address these issues by focusing on hard breakdown (HBD) and investigating the stochastics of the recovery phenomena. The results and analyses of this phenomenon will be helpful in ensuring improved control of the forming process for resistive switching devices, which is at present, quite a challenge to precisely control.

The sequence of this study is as follows. Section 2 introduces the sample fabrication and characterization conditions used for stressing. In Section 3, we plot the recovery trends observed during RVS tests and assess the stochastics of the breakdown and recovery events in the Weibull plot and provide a strong case for the use of the defect clustering model. Finally, Section 4 concludes with a summary of the results and presents key ideas worth investigating further.

2. Experimental setup and characterization approach

Devices under test were MOS capacitors with HfO_2 gate dielectric. A 4.5 nm thick HfO_2 was grown by an atomic layer deposition (ALD) system on an n-type Si substrate. Post deposition annealing (PDA) was conducted in an N_2 ambient for 10 min at 700 °C. Au/Cr electrodes were

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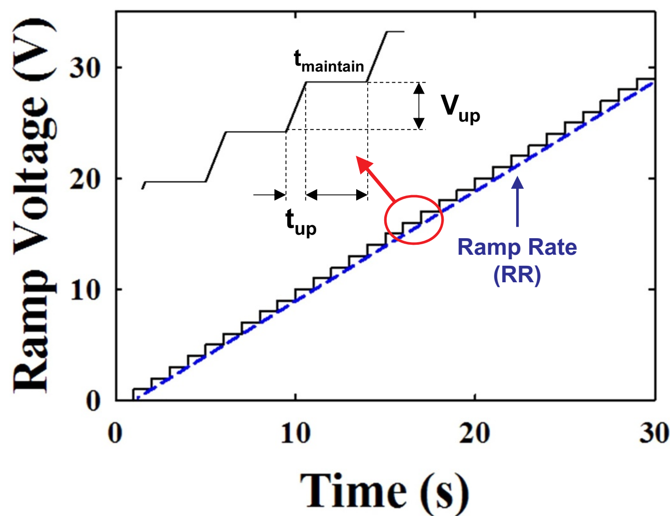

Fig. 1. Illustration of the voltage-time evolution trend in the pulse mode ramped voltage stress measurement (without any sense duration at low voltage) setup for the devices tested in this study. The desired ramp rate is chosen by controlling $t_{maintain}$.

deposited by e-beam evaporation and patterned. Circular electrodes with a radius of 40 μm were patterned to form the device under test (DUT). These circular devices were used for most of the tests, with the exception of Fig. 6, wherein the DUTs were 80 μm × 80 μm in area. The electrical measurements were conducted using the Keithley® SCS 4200 setup for temperatures ranging from 300 K to 400 K. Ramped voltage stress (RVS) breakdown tests were conducted with different ramp rates taking advantage of the pulse mode unit for statistically significant and time efficient sample size analysis. The pulse mode unit provided a more precise and stable ramp rate during RVS test than the conventional method. Fig. 1 illustrates the voltage-time evolution trend in our pulse mode measurements. The voltage step rise time (t_{up}) is 40 ns and the duration of fixed stress ($t_{maintain}$) depends on the desired ramp rate. Values for $t_{maintain}$ range from 100 μs to 0.4 s.

3. Results and discussion

3.1. Observed hard breakdown recovery trends

Typical *I-V* traces obtained from several identical devices during the RVS tests are plotted in Fig. 2, where all the devices have the same geometry, structure and process flow. The ramp rate (RR) here is set to be 10 mV/s. As can be seen from the figure, while for some devices, the first HBD is the only event that occurs, there are other devices where the HBD event recovers significantly by 2–3 orders of magnitude, following which, another HBD event occurs at a higher voltage. Quite a number of devices show up to 2–3 recovery events which confirms that HBD recovery is a repeatable phenomenon that is observed and deserves to be analyzed further.

When several 40 μm radii circular MOS capacitors were tested, observations reveal that the frequency of HBD recovery events varied quite a lot from sample to sample, also depending on the ramp rate of choice. Fig. 3 plots the number of such devices, which showed one or more recovery events. We do observe a lower probability of observing increasing number of recovery events as expected. Also, the probability of recovery heavily depends on the ramp rate, with slow ramp rates giving rise to much higher probability of recovery, as the filament has enough time and sufficient thermal budget to rupture and re-create an oxide barrier that causes conductivity to drop.

For devices that showed multiple recovery (REC) events, we further analyzed the dependence of voltage to subsequent HBD events ($V_{BD\text{-}2}$, $V_{BD\text{-}3}$, …, $V_{BD\text{-}n}$) on the magnitude of current drop after previous recovery ($I_{HBD\text{-}1}/I_{REC\text{-}1}$, $I_{HBD\text{-}2}/I_{REC\text{-}2}$, …, $I_{HBD\text{-}(n-1)}/I_{REC\text{-}(n-1)}$). Here, I_{HBD} and I_{REC} refer to the current in the stack just before and just after the recovery event, respectively and n refers to the cycle of breakdown and recovery (the first BD event on a fresh stack corresponds to $n = 1$). Fig. 4 shows the scatter plot of this dependency and we notice a strong positive correlation of the voltage needed for the next HBD on the extent of recovery of the previous HBD event (as illustrated by the elliptical contour in the plot). This implies that in most cases, it is the same breakdown spot that repeatedly switches ON and OFF. In other words, most of the subsequent BD and REC events tend to occur at the location of the very first HBD event which is natural to expect because the very first BD event is catastrophic enough to create enough damage in the oxide that cannot be "fully repaired". This is similar to the observation that the SET voltage (defined as the voltage at which resistance state shifts from high to low resistance reversibly in resistive switching memory) is always lower than the forming voltage in RRAM devices. There are a few outliers (shown in Fig. 4) that may however involve nucleation of new HBD spots in the device given its large area and finite possibility of having multiple weakest link locations due to microstructural variations; however, the numbers are quite small. Note in Fig. 4 that we are collectively analyzing the V_{BD}–I_{HBD}/I_{REC} values without examining their evolution over different cycles in any given device. This is because breakdown and recovery are random and stochastic phenomena that do not exhibit a clear pattern as a function of different cycles of recovery. The scatter plot in Fig. 4 in fact represents the data collected over several arbitrary BD-REC cycles in many different device units within a single wafer.

3.2. Statistical nature of first hard breakdown event

A Weibull plot of the voltage to first HBD event ($V_{BD\text{-}1}$) is shown in Fig. 5(a). It is well known that the Weibull distribution is the standard choice for describing the statistics of oxide breakdown events in SiO_2 and HfO_2. However, we observe a poor representation of the data when the Weibull model is used. This suggests that the statistical nature of the BD needs to be further investigated.

The defect clustering model was recently proposed by Wu et al. [11] to capture the process variability induced oxide thickness variations and line edge roughness on the TDDB statistics of middle of line (MOL) and back-end of line (BEOL) low-κ structures. The cumulative density function for the cluster model may be expressed by Eq. (1) below where η and β have the same meaning of mean voltage to BD and the Weibull slope (shape factor), while the additional factor, α_C, is referred to as the cluster factor. In effect, the clustering model is just a generalization of the Weibull model and when $\alpha_C \rightarrow \infty$, there is no clustering effect and the BD events are "completely random" based on the Poisson behavior that takes us back to the Weibull distribution.

$$F(V_{BD}) = 1 - \left(1 + \frac{1}{\alpha_C}\left(\frac{V_{BD}}{\eta}\right)^{\beta}\right)^{-\alpha_C} \quad (1)$$

When the cluster model was used to fit the data, we observe a much better fit as shown in Fig. 5(b). The value of α ranged between 0.2 and 0.4 suggesting that there is significant amount of defect clustering possibly due to the variations in the oxide thickness or microstructural effects in HfO_2 due to localized defect generation preference in and around the grain boundaries of the polycrystalline dielectric.

We further analyzed the dependence of Weibull slope on the ramp rate (Fig. 5(c)) and there was no clear dependence observed. This is in line with previous observations that the Weibull slope is insensitive to the voltage bias in constant voltage stress (CVS) TDDB experiment [12]. Using the equivalence relationship between RVS and CVS measurements for TDDB as established by Kerber et al. [13], where n is the voltage power law exponent obtained through a linear fit of log($V_{BD\text{-}63\%}$) versus log(RR) (Eq. (2)), the Weibull slope for CVS was estimated

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