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Life prediction methodology of system-in-package based on physics of failure

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ABSTRACT

With the dramatic development of microelectronics technology, System-in-Package (SiP) becomes a brand-new direction for the More than Moore's law. In order to satisfy the demand of small-size, multi-function and high-performance, complex structures and variable materials are applied in SiPs, which introduce many reliability problems. To implement reliability qualification and health assessment, a life prediction methodology of SiP based on physics-of-failure (PoF) is studied in conjunction with simplified life cycle profile. In this paper, typical structures of SiPs, such as dies, components, interconnects are evaluated. And related PoF mechanisms, such as time dependent dielectric breakdown, electro-migration, die attach fatigue, thermal cyclic fatigue and etc., are considered. The inputs of the methodology contain hardware information and lifecycle profile. The hardware information of SiPs includes materials types and structures size. Lifecycle profile provides environmental conditions that the SiPs should experience. Based on these inputs, thermal distributions and stress-strain distributions of the SiP are analyzed by finite element analysis (FEA) tools. With the utilization of PoF models, lifetime matrix of the SiP is obtained. The output of the methodology is the lifetime matrix to predict lifetime of the SiP. Finally, a case study is done to guide engineering applications.

1. Introduction

System-in-Package (SiP) integrates multiple chips, components and their connections in a package to form a microsystem. With increasing demands for functional integration, SiP becomes a brand-new direction for the More than Moore's law. SiP incorporates various technologies into one package, shown as Fig. 1 [1]. Consist of complex materials and structures, SiP is faced with several reliability challenges.

Previous research was focused on the reliability of SiP and its typical structures. Many studies were done for the lifetime predictions of these structures. Lu H analyzed the reliability of flip chip designs using computer simulation [2]. Y Li reviewed the Physics of Failure (PoF) models of wire bond interconnects and proposed a new damage-based crack propagation model to evaluate the lifetime of the wire bond interconnects [3]. Many studies only aim at the single structure in SiPs, but they cannot evaluate the comprehensive lifetime of SiPs. Based on PoF models, Farley D presented a PoF approach for SiPs, analyzed potential failure mechanisms of RF SiPs and predicted lifetime of multi-technology SiPs [4]. Utilizing PoF approaches, the lifetime of SiPs can be predicted rapidly and credibly.

In this paper, typical structures of SiPs, such as dies, components, interconnects are evaluated. And related PoF mechanisms, such as time dependent dielectric breakdown (TDDB), electromigration, die attach fatigue, thermal cyclic fatigue are considered.

The inputs of the methodology contain hardware information and lifecycle profile. The hardware information of SiP includes materials and structures parameters. Lifecycle profile provides environmental conditions that the SiPs should experience.

Based on these inputs, thermal distributions and stress-strain distributions of the SiP are analyzed by Finite Element Analysis (FEA) tools. With the utilization of PoF models, lifetime matrix of the SiP is obtained. The output of the methodology is the lifetime matrix to predict lifetime of the SiP. Finally, case study is done to guide engineering applications.

2. Basic theories

2.1. Failure mechanisms of SiPs

The SiP is made up of dies, components and interconnects. Silicon chips with different functions are mounted on the substrate, and electrical connection to the lead frame is achieved by wire bond, flip-chip or solder joints. The representative construction of SiP is shown in Fig. 2.

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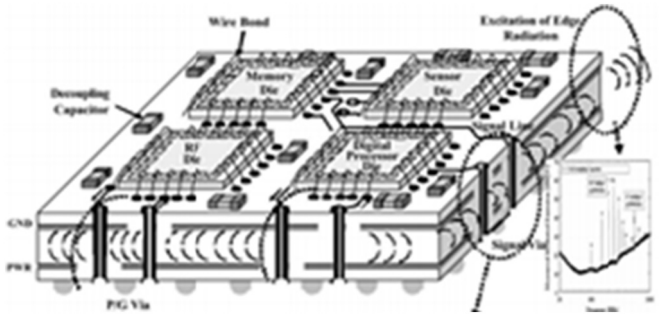

Fig. 1. Planar Multichip Module SiP [1].

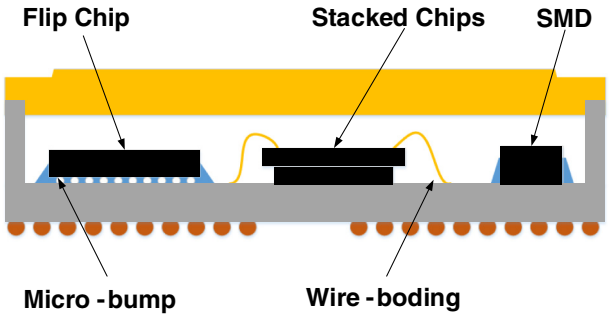

Fig. 2. Representative Constructions of SiP.

As mentioned above, SiPs have complex struc-tures that cover a variety of interconnects. So, failure mechanisms of SiPs are complicated and various, which are listed as Fig. 3.

2.2. PoF models

PoF models are broadly applied in lifetime evaluation of electronics, which can obtain lifetime of different failure mechanisms respectively. PoF models for SiP are divided into Front End of Line (FEoL) failure models, Back End of Line (BEoL) failure models and Packaging/Interfacial failure models according to different process stages. Maturity PoF models of partial failure mechanisms are reviewed as Table 1 [5].

Table 1
Common PoF models of SiPs [5].

Process stage	Failure mechanism	Failure model
FEoL	TDDB	E model 1/E model V model
	Hot carrier injection (HCI)	N-channel model P-channel model
	Negative bias temperature instability (NBTI)	NBTI model
BEoL	TDDB	E model 1/E model $E^{1/2}$ model
	Electromigration (EM)	Al EM model Cu EM model
	Corrosion	Reciprocal exponential model Power-law model
	Stress migration (SM)	Al SM model Cu SM model
Packaging	Fatigue	Coffin-Manson model [6] Norris Landzberg model
	Interfacial failure	Paris Law model

Based on PoF models, times to failure (TTFs) of SiPs for different failure mechanisms under BEoL, FEoL and Packing can be predicted, which are the foundations of life prediction methodology.

2.3. Competing failure rule

A variety of failure mechanisms and modes exist in SiPs with complex materials and structures. Competing failure rule can be used to analyze multiple failure mechanisms and give the weakness of the system. Lifetimes for all failure mechanisms are analyzed in competing failure process. If any of the failures occurs, other failures will not occur and the cause of system failure is failure mechanism with shortest lifetime [7]. From the competing failure rule, the time to failure (TTF) of a SiP for a life profile is expressed as Eq. (1).

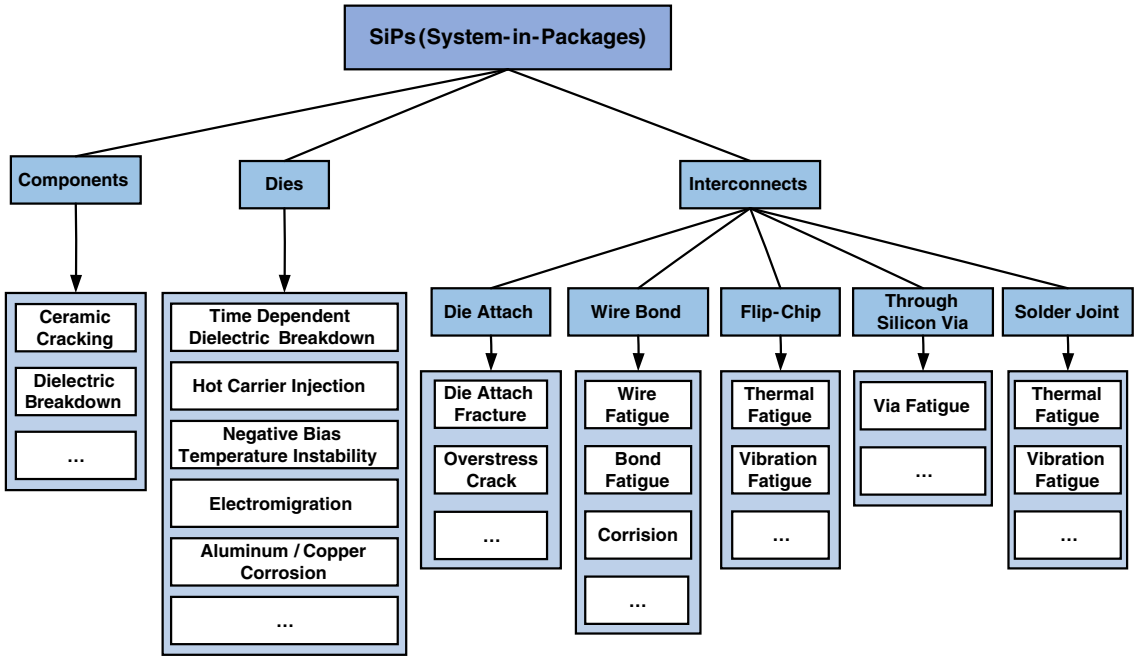

Fig. 3. Failure Mechanisms of SiPs.