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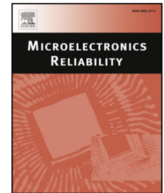
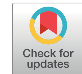


Unified view on energy and electrical failure of the short-circuit operation of IGBTs



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ABSTRACT

This work investigates the relation of the two destruction modes, the so-called *energy destruction* and the *electrical destruction*, during short-circuit operation of an Insulated Gate Bipolar Transistor (IGBT). The critical energy as a function of the short circuit current reveals a kink indicating the transition between two different failure modes. The failure signatures show that energy destruction takes place at lower currents and electrical destruction at higher currents. This supports the hypothesis that there is a huge current range with non-destructive filaments at low dc-link voltages. For both destruction mechanisms, the final failure occurs locally. For the energy destruction, the current crowding happens very late during the runaway itself, whereas in the case of an electrical destruction, filaments are formed mainly by an electrical mechanism leading to a stronger local self-heating. Both mechanisms take place far above the safe operating area of the chip.

1. Introduction

Short-circuit (SC) ruggedness is the capability of a transistor to withstand both a high voltage and a high current for a certain timeframe (e.g. 10 µs). Such a situation can occur if an inductive load is short-circuited, as exemplarily drawn for a simple H-bridge topology in Fig. 1, left. Depending on the status of the IGBT at the point in time a short circuit occurs, one can distinguish between different types of SCs [1]:

- SC type I: The IGBT is initially in blocking state and turns on into an existing SC of the load.
- SC type II: The IGBT is initially in conduction mode. During this phase the short of the load takes place [2].
- SC type III: the antiparallel diode conducts the current initially [3].

A second important parameter for the short-circuit stress is the stray inductance L_{stray} during SC events which is determined by the location of the short in the system. Furthermore, other parameters such as the emitter inductance and possible clamp circuits have a strong impact on the device ruggedness. However, in this work the focus is on the intrinsic SC ruggedness of the chip. The link between the intrinsic SC properties and the SC ruggedness under specific test conditions can be understood by analysing the transients of the collector current I_{C} and the collector and emitter voltage V_{CE} together with a destruction limit of a chip in an I_{C}-V_{CE}-phase diagram as it was done in reference [12] (Fig. 2). Beside the classical SC failures, the paper includes also two special SC turn-off destruction modes which are the static clamping failure and the overcurrent turn-off destruction during a fast turn-off in a transient low-voltage state.

From the chip design point of view, there are two different internal SC destruction mechanisms that have to be distinguished. At first, a so-called *energy* (or *thermal*) *destruction* is characterized by a critical energy $E_{\mathrm{crit,therm}}$ that the chip is able to dissipate during an SC event without destruction [4, 5, 16]. In addition, a destruction caused by current filaments can take place, which is called *electrical* or *current destruction* [6–13].

Fig. 3 shows photographs of two 1200-V IGBT chips of the same type with aluminium bond wires on the front side. Despite the fact that the left chip was destroyed by an energy destruction and the right chip by an electrical destruction, the failure picture is on a macroscopic view very similar. In both cases there is a local melting of the metallisation and the silicon in the active area. The only reason that the underlying destruction mechanism is known, is that the chips were tested with several SC pulses with a fixed dc-link voltage V_{dc} starting at a fixed gate-emitter voltage (V_{GE}) and increasing the pulse duration in very small steps of 0.2 µs until the device failed. The break between the pulses was chosen in such a way that the chip temperature declined

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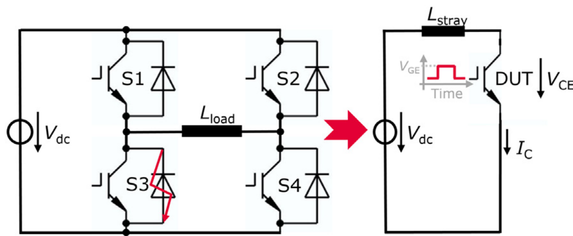

Fig. 1. Left: simple H-bridge topology with a SC of the load. Right: simplified test circuit for an SC type I.

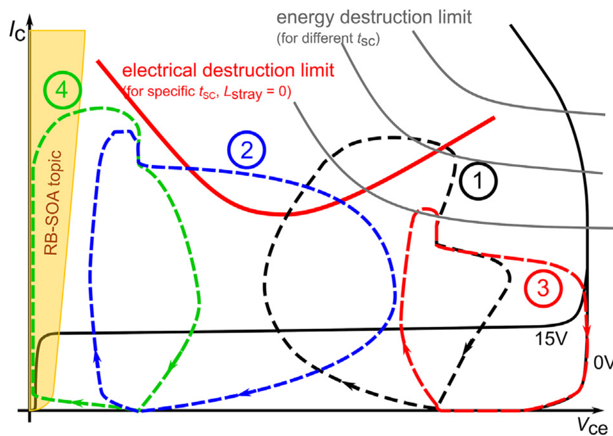

Fig. 2. Schematic view of the I_C-V_{CE} phase diagram with the 15 V- and 0 V-output characteristic, the energy destruction limit, the electrical destruction limit and the transient curves of the different SC events corresponding to the four electrical failure modes: 1-pulse failure, 2-turn-off failure, 3-static clamping failure, 4-fast turn-off in a transient low-voltage state [12].

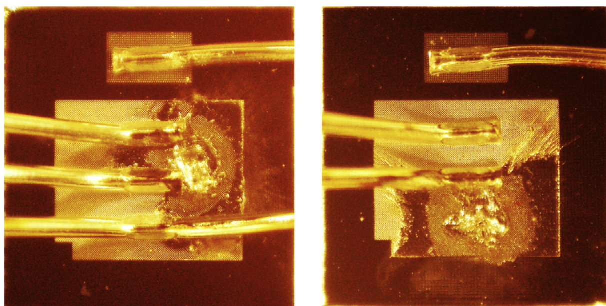

Fig. 3. Photographs of two 1200 V IGBTs destroyed during SC pulses with V_{GE} = 23.5 V, t_{sc} = 17.5 µs and V_{dc} = 600 V (left) and V_{GE} = 30 V, t_{sc} = 8.5 µs and V_{CE} = 400 V (right).

before each pulse to its initial value of 25 °C. For the left chip in Fig. 3, this procedure led to a thermal runaway of the leakage current a few 100 µs after the pulse indicating a thermal destruction. In the other case, the chip was destroyed very shortly after SC pulse. Since the left chip survived a much higher energy, current and voltage level seem to be decisive for this electrical destruction.

The purpose of this paper is to investigate the transition between the regime in which the chip fails due to an energy destruction and the regime with an electrical destruction. This is done by an experimental analysis of the dependency of the critical energy on the SC current and by device simulations. In this context the temperature dependency of the electrical destruction is analysed.

2. Impact of design parameters

Many parameters of the vertical design of an IGBT have a contrary

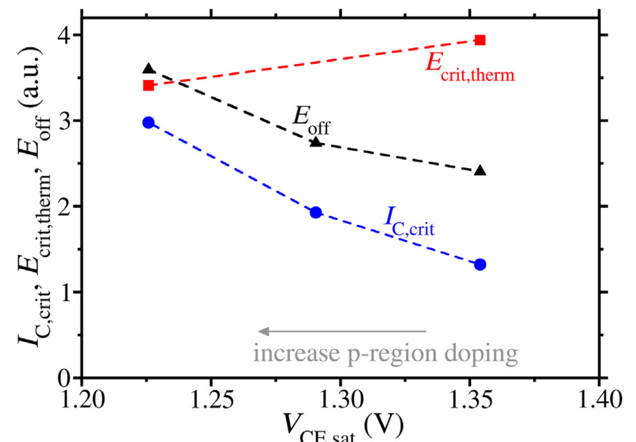

Fig. 4. Critical SC current $I_{C,crit}$, critical SC energy $E_{crit,therm}$ and turn-off losses E_{off} depending on the on-state voltage $V_{CE,sat}$. Three chip types with different p-region dopings were measured.

impact on energy and electrical SC failure. One example is the doping of the collector-side p-region. The p-region doping determines the ratio between the on-state losses represented by $V_{CE,sat}$ at nominal current and the turn-off losses E_{off} (Fig. 4). The higher the p-region doping, the more electron-hole plasma is stored in the drift region during conduction resulting in lower $V_{CE,sat}$ and higher E_{off}. High plasma is beneficial for low frequency operation, whereas a low plasma density leads to optimized overall losses in high frequency applications. In addition the p-emitter doping affects also the turn-off softness and the SC ruggedness. A decrease of the p-region doping level slightly increases the ruggedness against an energy destruction. On the other hand, a higher p-region doping can strongly improve the electrical SC ruggedness [6], Fig. 4.

With a lower chip thickness the heat capacity of the silicon is reduced leading to a lower thermal SC ruggedness [5], but an increased electrical SC ruggedness. The higher the doping level of the field stop layer, the lower is the electrical short-circuit ruggedness. The thermal SC ruggedness can be slightly higher.

Advanced design concepts such as the Injection Enhanced Floating Emitter (IEFE) [15] structure decouple the trade-off between energy and electrical failure and therefore allow an improvement of the withstand capability against both at the same time.

3. Test method and test chip

The right part of Fig. 1 shows the circuit used to characterize the short-circuit ruggedness applying a SC type I to an IGBT. It consists of a dc-link voltage source, a stray inductance L_{stray}, the DUT and a control circuit for the IGBT circuit. To characterize the energy destruction limit, the DUT is measured at high temperature, with a high dc-link voltage V_{dc}, a typical L_{stray} and a typical gate-emitter voltage V_{GE}. The pulse width t_{sc} is increased stepwise (e.g. 0.2 µs) until the IGBT fails. However, the characterization of the electrical SC ruggedness is usually done with a typical t_{sc} and a fixed V_{dc} by increasing V_{GE} stepwise (e.g. 0.2 V) until destruction. For most modern IGBTs low temperature is more critical with respect to destructive V_{GE}. Therefore, the measurements of the critical V_{GE} and the corresponding critical current of the 1200 V test chip with trench technology used for this work were measured at 25 °C. The resulting destruction limit has a characteristic minimum at a medium V_{CE} (Fig. 5), where V_{CE} denotes the voltage drop at the DUT in the quasi-stationary SC phase, which is usually characterized by a slight decrease of I_C caused by thermal heating in the channel area. For the small IGBTs used for this study V_{CE} almost equals V_{dc}.

The increase of the destruction current with voltage (600 V towards

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