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High resolution observation of defects at SiO_2/4H-SiC interfaces using time-resolved scanning nonlinear dielectric microscopy

Y. Yamagishi*, Y. Cho

Research Institute of Electrical Communication, Tohoku University, 2-1-1, Aoba, Sendai 980-8577, Japan

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ABSTRACT

High resolution observation of density of interface states (D_{it}) at SiO_2/4H-SiC interfaces was performed by time-resolved scanning nonlinear dielectric microscopy (tr-SNDM). The sizes of the non-uniform contrasts observed in the map of D_{it} were in the order of several tens of nanometres, which are smaller than the value reported in the previous study (> 100 nm). The simulation of the tr-SNDM measurement suggested that the spatial resolution of tr-SNDM is down to the tip radius of the cantilever used for the measurement and can be smaller than the lateral spread of the depletion layer width.

1. Introduction

Silicon carbide metal–oxide–semiconductor field-effect transistors (SiC-MOSFETs) are key devices in the field of power semiconductor devices and have been widely investigated to realize high voltage and low energy loss power devices [1–3]. For further improvement of the performance and reliability of SiC-MOSFETs, reduction of defects at the SiO_2/SiC interfaces is essentially important. While the current issues of SiC-MOSFETs such as low mobility and instability of threshold voltages are usually associated with the defects at the SiO_2/SiC interfaces [4–6], fundamental understandings on the nature of the interface defects are still missing.

To investigate the density and energy depth of the interface defects, deep level transient spectroscopy (DLTS) is a powerful technique [7–10]. While typical DLTS measurement usually employs a MOS capacitor and consequently is not capable of analysing the spatial distribution of the interface states, the additional function to visualize the spatial distribution is hopeful to allow obtaining information on the properties of the interface states from another point of view [11–13].

Based on this idea, we recently developed the measurement system to perform the DLTS measurement using a cantilever and visualized the distribution of interface states at nanoscales [14]. Unlike common DLTS measurements which require preparation of a MOS capacitor sample, the developed technique can be performed on SiO_2/SiC samples without an electrode, enabling to reduce the time needed for the evaluation of the interface quality. The current measurement system is based on time-resolved scanning nonlinear dielectric microscopy (tr-SNDM), which is a capacitance microscopy with a high capacitive sensitivity and an excellent time resolution [15]. In our previous study, we reported that non-uniform contrasts with the scale of several hundreds of nanometres were observed in the map of the density of interface states (D_{it}) of SiO_2/SiC samples [15]. However, the reported spatial resolution was not sufficiently-high compared to the expected sizes of the clusters of the excess atoms at the SiO_2/SiC interfaces [16]. One of the main reasons for the poor spatial resolution in the previous study was that we employed a cantilever with a relatively-thick tip radius (125 nm). Because the spatial resolution of tr-SNDM is influenced by factors such as the tip radius of the capacitance probe and the oxide thickness of the sample, refining these parameters are essential for visualizing finer structures in the distribution of interface states.

In this work, we perform mapping of D_{it} with a higher spatial resolution using a cantilever with a tip radius of 25 nm and employing a SiO_2/SiC sample with an oxide thickness of 10 nm. The spatial resolution of tr-SNDM is also discussed based on the results obtained by TCAD simulation.

2. Principle of tr-SNDM

Fig. 1 shows the schematic of the measurement system. A pulsed voltage is applied to the sample and the capacitance transient is measured using an SNDM probe, which can measure the variation in capacitance down to 2×10^{-22} F/Hz$^{1/2}$ [17]. After the output of the SNDM probe is down-converted to an intermediate frequency signal (e.g., 30 MHz) and recorded using a high-speed digitizer, the capacitance transient is derived by digitally-demodulating the frequency-modulated signal [15]. Finally, the density and the energy depth of the

* Corresponding author.
E-mail address: yamagishi@riec.tohoku.ac.jp (Y. Yamagishi).

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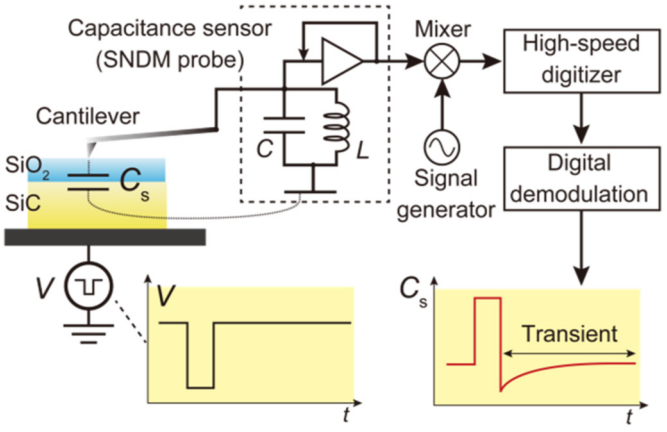

Fig. 1. Schematic of tr-SNDM measurement.

interface states are obtained by analysing the amplitude and the decay time constant of the capacitance transient based on the theory of Fourier DLTS [18].

3. Material and methods

The sample characterized in this study consisted of a 10-nm-thick oxide layer formed by dry oxidation at 1200 °C on an n-type 4H-SiC (0001) epilayer. The thickness of the oxide layer was controlled by adjusting the oxidation time. The sample was subsequently treated by post oxidation annealing (POA) at 1250 °C in an NO-containing gas. When tr-SNDM measurements were performed, the high level and the low level of the pulsed voltage were set to 0 V and −5 V, respectively. The pulse width was configured to be 5 μs. The capacitance transient was measured for 40 μs after turning-off the pulse and the exponentially-decaying component with the decay time constant of about 17 μs was extracted and analysed by Fourier DLTS. In the analysis, the capture cross section of the interface states was assumed to be 1×10^{-16} cm^2. The energy depth E_T of the interface states evaluated in this study was 0.35 eV from the conduction band edge of SiC (E_C).

4. Results and discussions

4.1. Observation of defects at SiO_2/4H-SiC interfaces by tr-SNDM

Fig. 2(a) shows the D_{it} map obtained by tr-SNDM. The values of D_{it} are roughly in the range between 1.0 and 6.0 × 10^{12} cm^{-2} eV^{-1}. Non-uniform patterns are observed in the D_{it} map and the sizes of the clusters are in the order of several tens of nanometres, which are smaller than the values reported in the previous study (> 100 nm) [15]. A typical topographic image of the same sample is shown in Fig. 2(b). Because the scratch-like features observed in the topographic image are clearly different from the contrast patterns observed in the D_{it} map, the inhomogeneous pattern in the D_{it} map is not due to a topographical artifact. A line profile extracted from the white line indicated in the D_{it} map is also shown in Fig. 2(c). The width of the transition region between a high-D_{it} area and a low-D_{it} area is about 32 nm and roughly in agreement with the tip radius of the cantilever. The reason for the improved spatial resolution is considered to be mainly attributed to the reduced tip radius of the cantilever, as discussed in the next section. We think that one of the possible candidates for the observed non-uniformities may be associated with C-related defects, which were investigated in previous studies on SiO_2/4H-SiC interfaces [16,19]. We note that it is likely that the observed charge non-uniformities at the SiO_2/SiC interfaces influence the carrier transport characteristics of SiC-MOSFETs because it is known that the non-uniformities of the interfacial charges degrade the carrier transport in the inversion layer of Si-MOS transistors [20–22].

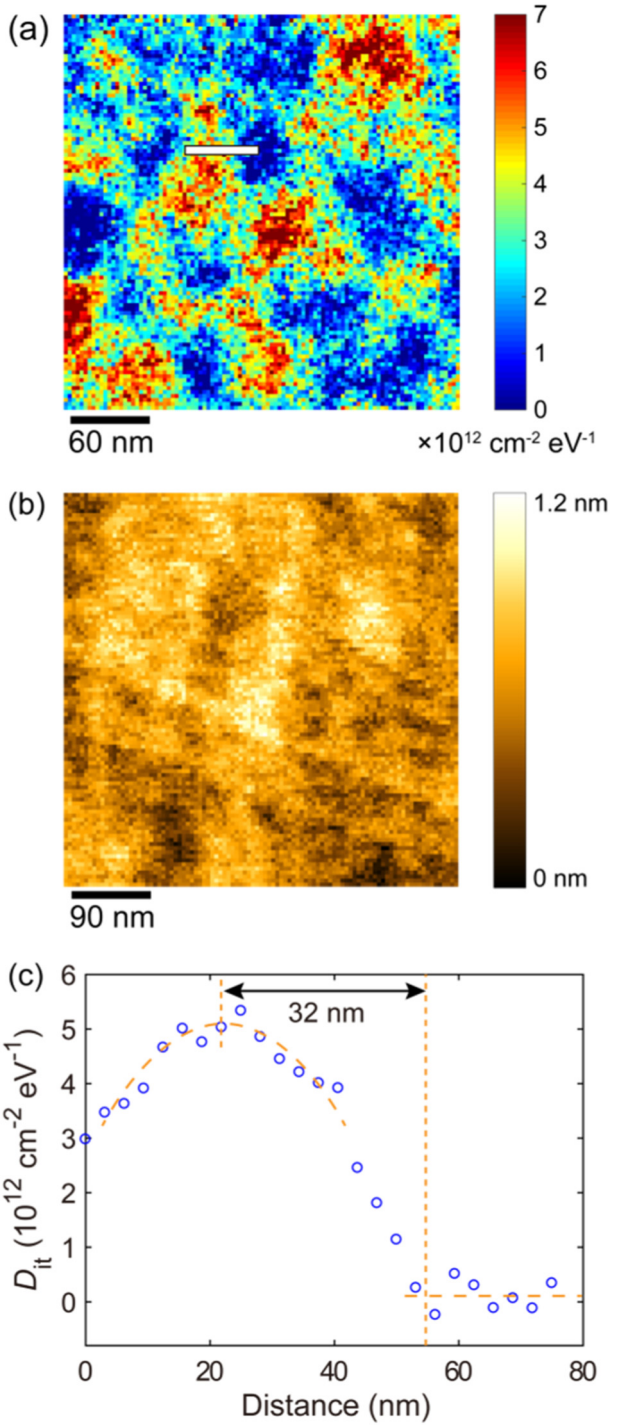

Fig. 2. (a) D_{it} map of the SiO_2/SiC sample obtained by tr-SNDM. (b) A typical topographic image obtained at a different point of the same sample. (c) A line profile of D_{it} extracted from the white line indicated in (a).

4.2. Simulation of tr-SNDM

To investigate the spatial resolution of tr-SNDM, distribution of trap occupation function at the SiO_2/SiC interface during the tr-SNDM measurements were calculated using a TCAD simulator (ATLAS). The schematic illustration of the geometry used in the simulation is shown in Fig. 3(a). The energy distribution of D_{it} that is defined based on the experimental results obtained by macroscopic constant-capacitance