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Exploitation of Laser Voltage techniques for identification and complete characterization of a scan chain transition fail issue using the second harmonic approach

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ABSTRACT

This work presents a Failure Analysis case study related to a scan chain integrity issue. By using Laser Voltage Imaging and Probing (LVx) approaches, we have been able to localize a defect that was inducing a transition failure, detected during scan chain integrity test flow.

Laser Voltage Imaging (LVI) and Laser Voltage Probing (LVP) techniques were applied with the aim of both identifying and characterizing the first failing flip-flop of the chain, in order to understand the failure mechanism.

The relatively simple Design For Test (DFT) structure of the device, made of a single scan chain to address a large area of the digital logic, and the nature of the electrical behaviour did not allow the ATPG Scan Chain diagnostic to be accurate, leaving the failure identification task to the FA engineer with the help of classical optical techniques.

In this work we specially focused on the application of the two fault isolation techniques, to first, identify the failing flip-flop through dichotomy approach, investigating the macro failure mode through a second harmonic LVI analysis and finally characterizing this failure using LVP.

1. Introduction

Nowadays, MEMS sensors become a significant part of the microelectronic industry. Both consumer and automotive sectors are producing integrated circuits embedding such devices. The test case we are dealing with in this paper, is an accelerometer sensor that can be used in various fields, including consumer and automotive systems.

The MEMS sensor device includes a separate control ASIC die, embedded within the same package. The failure analysis study presented in this publication is related to this control ASIC.

The IC interface of the sensor is manufactured using a Bipolar-CMOS-DMOS (BCD) process that allows high level of integration. The device is factory trimmed to fine tune the sensing elements with regards to standardized acceleration excitations, in order to optimize the performance.

The acquisition chain is made of a C/V converter, a full-differential charge amplifier, a 2nd order Sigma Delta (SD) analog-to-digital converter and a digital core, which includes filtering, compensation and interpolation, control logic and SPI protocol generation functions.

This work focused on failure analysis case studies of the digital IC of the device using laser voltage techniques [1] to identify the first failing flip-flop of a scan chain showing a transition failure during the scan chain integrity test, and characterizing the failure mode of the highlighted failing cell.

Laser Voltage Imaging (LVI) and Probing (LVP) are two complementary failure analysis techniques based on laser interaction. LVI is a failure isolation technique that allows mapping the activity of transistors toggling at a specific frequency. It is used to address scan chain related defect by detecting the flip flop activity at different frequencies. LVP is a probing based technique that allows collecting waveforms running inside a transistor in order to compare it with simulation and/or a reference device.

2. Testing analysis

The device under investigation failed production final test. First verification has been performed by product engineering on the ATE (Automatic Test Equipment), to confirm the nature of the failure, which

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is related to a chain integrity issue, and more specifically to a so-called transition failure.

The electrical analysis performed through Actual Mode approach on the ATE showed an anomalous reading of the “pattern 0”, while emulating the scan chain in serial mode with a classical “0011” periodic signal. During reading, an anomalous “L-*H*-H-H” was measured, which differs from the expected “L-L-H-H” signal.

This type of failure mode could be modelled by a “fast-to-rise” fault model, where the data latched by the flip-flop seems to change in advance with respect to the latching clock.

The failure mode was characterized versus voltage, frequency and temperature, but the sample did not show any dependency on those parameters. This defect can be categorized as a “hard defect”, on which Dynamic Laser Stimulation approaches are not efficient to localize the defective structure.

The ATPG Scan Chain diagnostic result on this scan chain integrity issue did not provide good feedback, mainly due to the nature of the electrical failure. Both the score and the precision of the diagnostic process did not guarantee reliable level of confidence. Since the Design For Test structure is made of a single long scan chain, it is more difficult for the ATPG Scan Chain diagnostic software to generate clear and accurate results, when dealing with scan chain integrity issue.

3. Hardware setup and sample preparation

The unavailability of a product dedicated board with the footprint of the pogo-ring interface of our failure analysis laboratory digital tester forced us to realize a new interface, allowing the High Speed Digital Channels (HSD) to be provided to the Device Under Test (DUT).

A generic IDS format board (used for Laboratory Tester) was modified in order to connect high speed digital cables to the equipment specific board, where the DUT was placed in a specific socket for failure analysis.

Sample preparation was needed in order to allow the exposition of silicon back-side since Laser Voltage Imaging and Probing (LVx) techniques are backside approaches.

The sample was prepared by parallel lapping technique. Being a flip-chip device, the top of the package was thinned, with the aim of removing the moulding compound, thinning and polishing the silicon backside of the die. Unfortunately, due to the package and socket configuration, the Solid Immersion Lens (SIL) that is available on our LVI system (Meridian IV from Thermo Fisher Scientific) could not be used. All the analyses have been performed using air gap lenses only.

4. Electrical analysis and failure verification

Scan pattern has been received from the product engineer and loaded into a laboratory digital tester (Teseda V550). Small modifications have been performed on the digital scan pattern in order to meet the requirements of laser voltage techniques. In order to optimize LVI results, we need to get 50% duty cycles signals (clock and scan IN) and fully periodic signals over test loops. For LVP, an additional trigger signal has been generated in the test loop and will be used to define a time reference for waveforms reconstruction.

The modified scan pattern was run on the failing sample and the failure mode confirmed. Resulting waveforms are presented in Fig. 1.

5. Fault isolation setup and results

Fault isolation was initially started by performing Photo Emission Microscopy (PEM) while looping on the test pattern [2].

The acquired photo-emission images did not allow to provide any potential failure location, since no significant difference could be observed while comparing with a reference device. In fact, since we are dealing with a transition failure, all flip-flops of the scan chain are still toggling due to clock and scan IN signals. So it is very difficult to detect

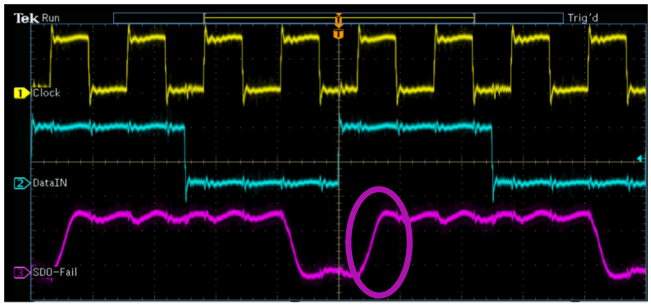

Fig. 1. – Data IN (Scan In) signal (Blue), SDO (scan-out) improperly latched on the second clock pulse of the period (pink circle), Clock signal (Yellow). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

any difference in the photo-emission coming from flip-flops before and after the defective structure. Moreover, since this failure mode is only visible in dynamic mode, it was not relevant to run static photo emission.

As next, another approach was evaluated, applying a different fault isolation technique, based on LVI and LVP. These techniques [3] are able to detect free carrier density variations underneath a functional transistor, by monitoring the variation of the reflected light of an incident continuous wave laser. Depending on the transistor state, the reflection and absorption of the active area will slightly vary. By using a very sensitive and high speed photodetector we can detect these small variations in the reflected beam.

The modulation of the reflected wave can be highlighted on a scanned image (LVI). While scanning the laser onto the area of interest, the reflected signal is transferred into a spectrum analyser set to a specific frequency (generally the clock or data in frequency). On the resulting LVI image, all transistors running at the frequency of interest will be highlighted. Several scans at various frequencies can be run to image all transistors running the clock and/or the data IN signal.

For Laser Voltage Probing, the laser beam will be parked to one specific location and the signal from the photodiode will analysed using an oscilloscope in order to reconstruct the waveform running into this transistor (Fig. 2).

LVx techniques can be used to both identify potential failure sites, through LVI mapping and characterize this highlighted location by probing all nodes using the LVP approach.

The signal provided as an input data to the device is a periodic square waveform with 50% duty cycle, reproducing the integrity chain test.

Scan (shift) clock has a frequency of 1 MHz, whereas the Data IN is 4 times less (e.g. 250 kHz), providing the “0011” bits, with a return-to-zero (RZ) clock pulse per bit. This choice has been done in order to avoid harmonics of the Data IN signal (750 kHz, 1250 kHz …) onto the clock frequency (1 MHz). This is a classical setup when dealing with LVI and scan chain integrity issues [4].

Fig. 3 shows an overview of the overlay of the scan chain nets to the layout. Fig. 4 is highlighting the first and the last flip-flop of the chain along with their connections to input and output pads respectively.

Because of the failure type (transition failure) we know that all flip flops of the scan chain are receiving the clock signal. By setting up the LVI system to detect the clock signal (running at 1 MHz), we can verify that a clock signal is present at all of them.

In the same way, a second LVI acquisition was run to look for the Data IN frequency (250 kHz). Both results are presented in Fig. 5 which contains both the clock (blue-pink) and the Data IN (yellow-orange) overlaid on top of the LSM reflected image.

As expected, we can observe Clock and Data IN LVI signals on all flip-flops activated by the test. No significant differences can be found on LVI signatures of different flip-flops of the same kind. We can clearly