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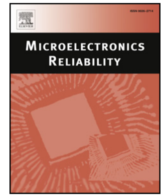

Complex automotive ICs defect localization driven by quiescent power supply current: Three cases study

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ABSTRACT

Quiescent current (IDDQ) test demonstrated over years its effectiveness in identifying the ICs failure root causes. In this paper three cases study are presented, all based on the use of IDDQ test during Emission Microscopy (EMMI). The DUTs analyzed, implemented in different technological solutions (BCD and BiCMOS), belong to the automotive market segment. In the cases here described the emission microscopy approach from both front and backside has been considered. Different physical analysis techniques have been used in order to characterize morphological marginalities or abnormalities. Results from the three cases should be good examples to prove how this kind of approach - fault isolation driven by IDDQ - is a powerful technique able to identify quickly and precisely failure root causes in high complexity ICs, independently of design and technology, and even when Automatic Test Pattern Generation (ATPG) is not available.

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Preferred track (please, tick one or number 1 to 3 tracks in order of preference: 1 = most suiting, 3 = least suiting).

[3] A - Quality and Reliability Assessment Techniques and Methods for Devices and Systems
[] B1 - Si Technologies & Nanoelectronics: Hot Carriers, High K, Gate Materials
[] B2 - Si Technologies & Nanoelectronics: Low K, Cu Interconnects
[] B3 - Si Technologies & Nanoelectronics: ESD, Latch-up
[1] C - Progress in Failure Analysis: Defect Detection and Analysis
[] D - Reliability of Microwave and Compound Semiconductors Devices
[2] E1 - Power Devices Reliability: Silicon and Passive
[] E2 - Power Devices Reliability: Wide Bandgap Devices
[] F - Packaging and Assembly Reliability
[] G - MEMS, Sensors and Organic Electronics Reliability
[] H - Photonics Reliability
[] I - Extreme Environments and Radiation
[] K - Renewable Energies Reliability
[] L - Modeling for Reliability
[] SS1 (Special Session) - Reliability in Traction Applications

1. Introduction

Automotive market requires more and more reliable ICs in order to reach the challenging target of zero fails in the field.

In this context, Failure Analysis of qualification failures and field returns has a key role in the achievement of this goal since, by using complex techniques, it is able to identify manufacturing “killer” faults and accordingly trigger the implementation of corrective actions in the production flow.

In this work three complex Failure Analysis cases on Automotive ICs are presented. They are based on different technologies, Smart Power BCD (Bipolar CMOS DMOS) and BiCMOS (Bipolar CMOS), and linked

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together by the anomalous absorption of Quiescent Current (IDDQ).

IDDQ is defined as the current consumption in CMOS circuit when all logic states have settled, and they are in steady state or quiescent mode [1].

By extension, in complex devices such as Smart Power BCDs and BiCMOS, IDDQ measurements have to take into account the bias of the analog stages: it can be defined as the IC current consumption when all the logic states have settled, all the internal analog current generators and voltage regulators are in steady state.

Literature and experience show that a number of CMOS typical physical defects (open circuit, floating gates, bridging defects, etc.) are not detectable by common voltage-based fault isolation techniques [2, 3] or by diagnosis based on Tester Automatic Patterns [4], while their localization requires a specific approach combining the measurement of quiescent current (IDDQ) with the emission microscopy (EMMI).

Moreover, the use of IDDQ and EMMI is not only an efficient way to identify physical defects in CMOS circuits. In fact, by its above definition, IDDQ also becomes an efficient parameter to localize defects on analog (Bipolar) stages.

However, the implementation of this approach is not an easy task, since it requires dedicated hardware able to run IDDQ test patterns, or equivalent complex setups able to replicate the IC steady state.

In fact, IDDQ test condition is usually defined by patterns automatically generated by software tools with a methodology named Automatic Test Pattern Generation (ATPG).

The three practical cases presented in this paper are aimed at proving how fault isolation driven by IDDQ is a powerful technique able to identify quickly and precisely failure root cause in high complexity ICs, independently of the design and the technology, even when Automatic Test Pattern Generation (ATPG) is not available.

2. Experimental

2.1. Electrical characteristics

The analysis of the first DUT in BiCMOS technology, called DUT1, required a logic tester to perform electrical failure verification and localization.

The Diagnostic Test Hardware Teseda Instrument [5] for lab activities was used.

The sequence of test modes allows testing of all the combinatory logic in different configurations, and measuring the value of the leakage current IDDQ strobing it in a certain timeframe of the test pattern.

By its definition, this parameter is strobed several times during the Test Program (usually 20 times) and its value, for good units, is around few nA.

For DUT1 two cases are presented (now called case A and case B).

The common symptom of the failing devices was “higher than normal IDDQ current”: its magnitude for defect-free circuits is almost null while current strobes for failing devices may reach several hundred of μA (see Fig.1).

The IDDQ measurement has been performed through 15 different IDDQ patterns for both the failing cases here presented. Several high leakage current have been observed with respect to the reference sample, as reported in Fig. 1.

For the electrical analysis of the second DUT (DUT2) in BCD9 technology, specific experimental set-up was implemented to obtain the electrical failure verification and localization for the failing IDDQ pattern. The selected IDDQ pattern was reproduced through bench static conditions and a custom validation board, not using dedicated dynamic tester.

The measurement confirmed high leakage current (hundreds of μA) with respect to the reference sample (almost null current).

The third DUT (DUT3) in BCD9 technology failed during digital scan test and showed an anomalous leakage current in IDDQ.

Since stack at pattern was failing, Tetramax [6, 7] was used to

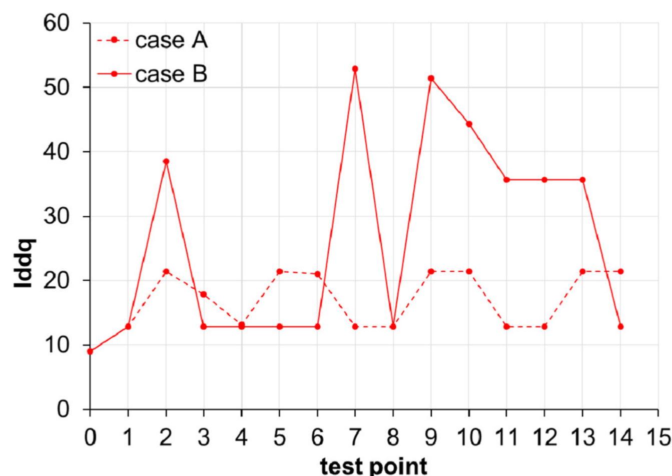

Fig. 1. Value of normalized IDDQ in the two practical cases for 15 vectors.

confirm electrical failure and localize possible failing cells in the digital circuitry.

High IDDQ leakage current was not reproduced by using a dedicated digital tester (as done for DUT2).

2.2. Fault localization

Considering the nature of the failure mode and the IC layout, Photon Emission Microscopy (EMMI) from backside has been judged the best technique of fault localization on the faulty ICs. The two samples belonging to DUT1 case were forced to stay in loop in higher absorption state (by using TESEDA dedicated pattern) showing an anomalous spot in a precise location inside the CMOS logic circuitry; this spot is not expected and not present in a reference good sample during IDDQ test.

The results are shown in Fig. 2.

After obtaining the information of the failing layout area, the analysis continued by means of CAD tools.

EMMI spot pictures have been overlapped onto the CAD layout (see Fig.3) in order to identify the failing block involved.

The aim of this step is to correlate the anomalous spot seen to possible physical anomalies on the dice – on the basis of the elementary structures present on the emission area – in order to choose the most appropriate physical analysis technique.

The overlapping of emission sites and CAD layout is reported in Fig. 3.

It is possible to observe that the emission site is related to a logic port gate driven by a signal internally generated for both units.

Two possibilitiehave been considered:

- The first, that a defect is affecting the polysilicon layer or the gate oxide layer belonging to the emitting CMOS;
- Secondly, an open circuit in the path of the signal (vias, metal, contacts or polysilicon layers) used to carry the internal signal to the emitting gate.

On the basis of these two hypothesis parallel lapping (combination of mechanical lapping and wet etches in order to selectively remove layers) has been chosen as physical analysis technique, since it allows to observe a wide portion of the layout.

In DUT2, due to the presence of RDL (Redistribution Layer) in BCD9, EMMI from backside was the selected technique to investigate the failed sample. The DUT showed an anomalous spot in a precise location inside the logic circuitry; this spot is not expected and not present in a reference sample during IDDQ test.

Results are shown in Fig. 4.

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