Microelectronics Reliability 88–90 (2018) 321–333

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Failure analysis on 14 nm FinFET devices with ESD CDM failure

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ARTICLE INFO

Keywords:
Electrostatic Discharge (ESD)
Failure analysis
14 nm FinFET
Metal gate

ABSTRACT

Electrostatic Discharge (ESD) is an important area for the semiconductor industry because ESD has an impact on production yield and product quality. ESD problems are increasing and have become challenging in the semiconductor industry because of the trends toward higher speed and shrinking in technology node. By continually shrinking the transistor with technology scaling, the process, circuit design, and failure analysis (FA) are getting more challenging. This paper is about FA on a 14 nm Fin-Field Effect Transistor (FinFET) device which has ESD failure after Charged Device Model (CDM) test. In most ESD failure FA, most of the time found Electrical Over Stress (EOS), the important is to understand which process layer or design causing the EOS. At the same time, this paper also discusses the difficulties faced, the FA technique used, the bottleneck of the 14 nm FinFET FA by old technology node FA equipment, and the FA findings. Finally, the ESD failure was identified with Scanning Transmission Electron Microscope (STEM)/Energy Dispersive Spectroscopy (EDS) analysis. The FA findings of the failure are related to the front end of line (FEOL), the metal gate of FinFET was fused with active, and the material in the metal gate was out-diffused.

1. Introduction

There is a growing interest in the effects of Electrostatic Discharge (ESD) on the performance of semiconductor integrated circuits (IC) because of the impact the ESD has on production yield and product quality. ESD problems are increasing and have become challenging in the semiconductor industry because of the trends toward higher speed and advancement in technology node. In advance technology node, a lot of critical items shrink such as metal spacing, gate oxide thickness, inter-metal dielectric (IMD) thickness, and etc. The advancement has created a lot of challenge toward the process, circuit design, and also failure analysis (FA). Today, there are three major stress methods which are widely used to describe uniform methods for establishing ESD withstand thresholds [1]. The commonly used stress model are 1) Human Body Model (HBM), 2) Charged Device Model (CDM), and System Level ESD (Machine Model). CDM test is a component level stress that simulates charging and discharging event that occurs in production equipment and processes. This paper will focus on FA on a 14 nm Fin-Field Effect Transistor (FinFET) device with ESD CDM failure. At the same time, this paper also discusses the difficulties faced, the FA technique used, the bottleneck of the 14 nm FinFET FA by old technology node (40 nm) FA equipment, and the FA findings.

2. Background and FA technique

A few package units were returned from customer site for FA after ESD CDM Qualification (QUAL) failure, those package has failed early stage voltage stress (< 100 V). The failure symptom is high leakage on input-output (IO) pins of ESD circuit for all failed units. Fig. 1 shows the current-voltage (IV) measurement on 1st, 2nd, and 3rd bad units. The IV results show high leakage on bad Unit#1 IO Pin 123 and Ohmic short on bad Unit#2 IO pin 131 compared with good dies. The packages were polished to die backside level to perform Electrical Failure Analysis (EFA) fault isolation with Thermally Induced Voltage Alternation (TIVA) analysis. TIVA analysis is one of the commonly used EFA technique to locate the leaky path by irradiating infra-red (IR) laser to a biased IC. Optical power from the laser is converted to thermal energy on conductive material and induces resistivity variation.

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https://doi.org/10.1016/j.microrel.2018.06.105
Received 24 May 2018; Received in revised form 24 June 2018; Accepted 28 June 2018

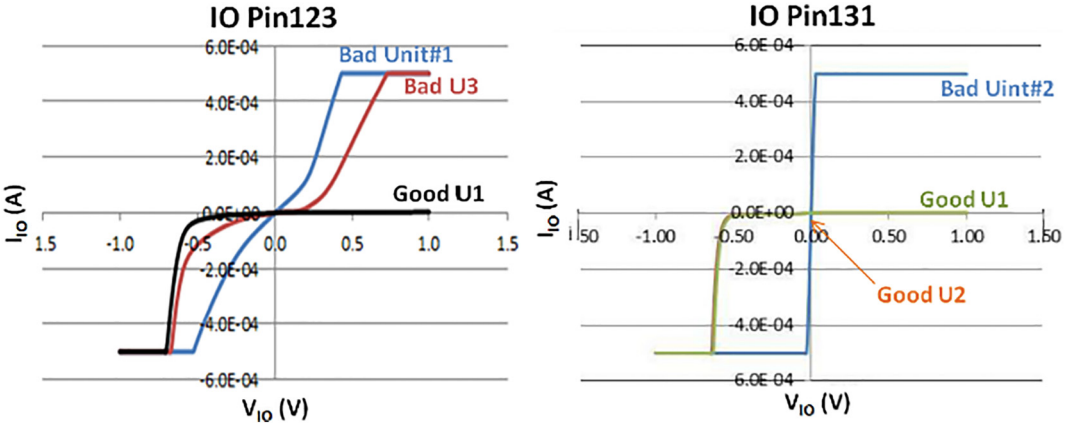

Fig. 1. IV measurement of IO pin that have leakage on Good and bad dies.

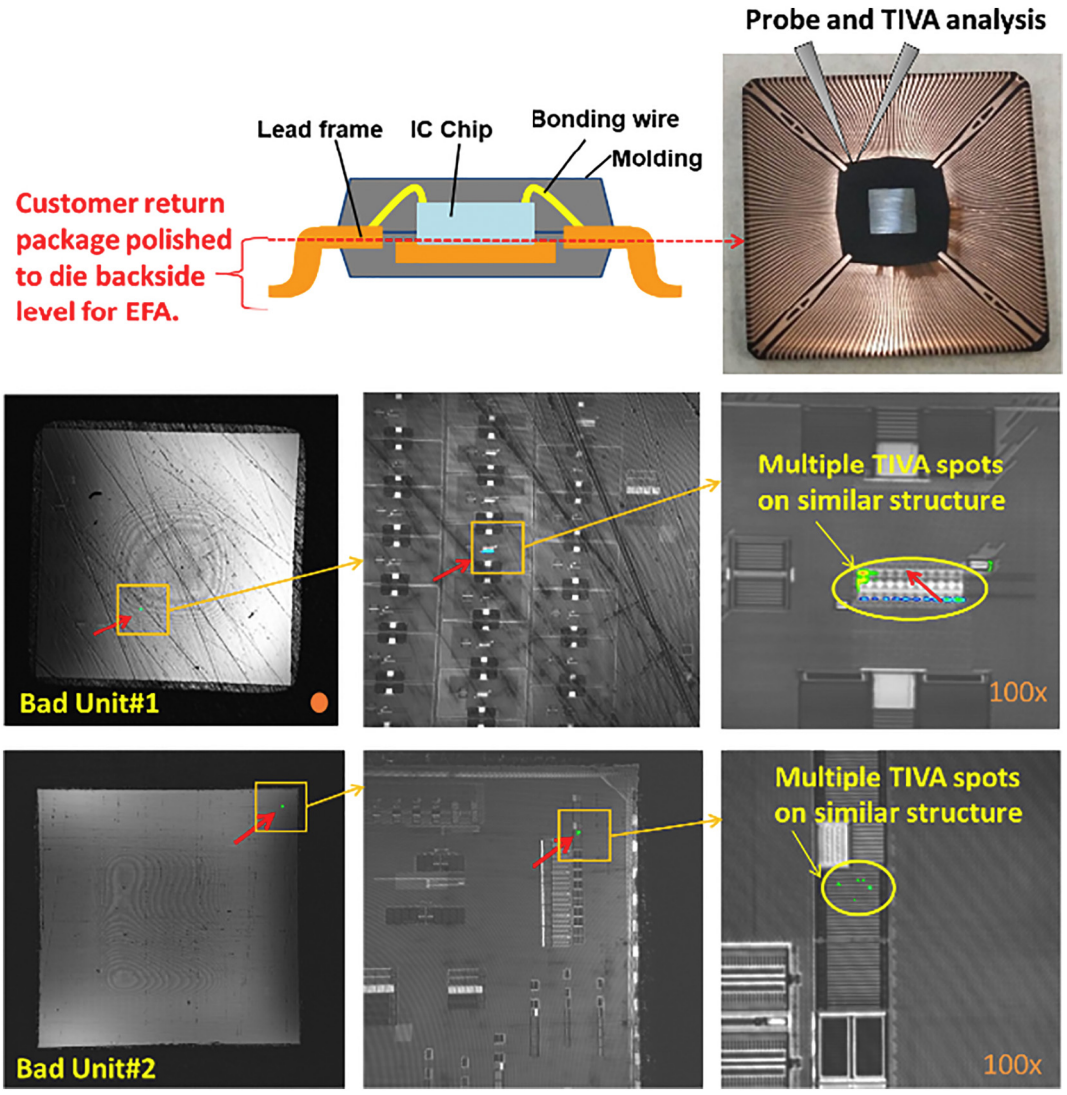

Fig. 2. TIVA result on polished package for short/leakage failure, Unit#1 and Unit#2.