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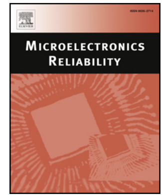
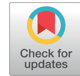


Impact of carbon impurities on the initial leakage current of AlGaN/GaN high electron mobility transistors



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ABSTRACT

We have systematically studied the origin of high gate-leakage currents in AlGaN/GaN high electron mobility transistors (HEMTs). Devices that initially had a low gate-leakage current (good devices) are compared with ones that had a high gate-leakage current (bad devices). The apparent zero-bias Schottky barrier height of bad devices ($0.4 < \phi_{B0} < 0.62$ eV) was found to be lower than that of the good devices ($\phi_{B0} = 0.79$ eV). From transmission electron microscopy (TEM) and electron energy loss spectroscopy (EELS) analysis, we found that this difference is due to the presence of carbon impurities in the nickel layer in the gate region.

1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) have a great potential to enable high power and high frequency electronics applications. While there has been some successful commercialisation of these devices, large scale market adoption has not yet been seen. This is partially due to an unclear understanding of the origin of low device fabrication yield and reliability, particularly of the origin of high gate-leakage currents [1].

High gate-leakage currents have been observed in devices after stressing under reverse bias at high temperatures [2]. Initially it was proposed that the increase in gate-leakage current is due to gate-edge degradation in the form of cracks, pits or grooves [3, 4]. However, later studies showed that this is not necessarily the case. Gate-edge degradation is not always accompanied by an increase of the gate-leakage current [5–9] and an increase of the gate-leakage current is not always accompanied by gate-edge degradation [10, 11].

More recently, an alternative explanation based on percolation path theory was proposed to explain increases in gate-leakage currents [10, 12]. This is consistent with the statistical distribution of this degradation. However, the nature of the physical defects associated with the formation of the percolation path is still unclear.

While there have been many studies of increases of gate-leakage due to stressing, there is still a limited understanding of the origin of initially high gate-leakage currents in unstressed devices (i.e. bad devices). This understanding is important as it could be used as the basis for process optimization and therefore could lead to further yield improvements. Furthermore, without screening these devices from reliability test data, an underestimate of the true reliability could result.

2. Experimental details

Fig. 1 shows the layer structure of the devices used in this work. The epitaxial layers were grown using metal organic chemical vapor deposition (MOCVD). Device fabrication was carried out using conventional device processing that involved a gate lift-off process. After fabrication, these devices underwent thermal aging at 225 °C for 500 h. Further details on the device dimensions and process parameters can be found in ref. [13].

We tested a total of 30 devices. 6 of these devices had a very high initial gate-leakage current density ($J_{Gate} > 5 \times 10^4$ A/m^2). We considered those to be 'bad' devices. The remaining had a very low leakage current density ($J_{Gate} < 2 \times 10^{2-}$ A/m^2), and thus we considered those to be 'good' devices. J_{Gate}-V_{Gate} curves for these devices are shown in Fig. 2.

Fig. 3 shows I_{Drain}-V_{Gate} curves of good and bad devices. We can clearly see that bad devices have a much higher initial drain leakage current than good devices. The threshold voltage of both types of devices is quite similar. Good devices have $V_{th} = -2.6 \pm 0.2$ V, while bad devices have $V_{th} = -2.5 \pm 0.3$ V. This suggests that there is no substantial difference in the trap level density below the gate.

Bad devices used in this study are already considered 'failed' as

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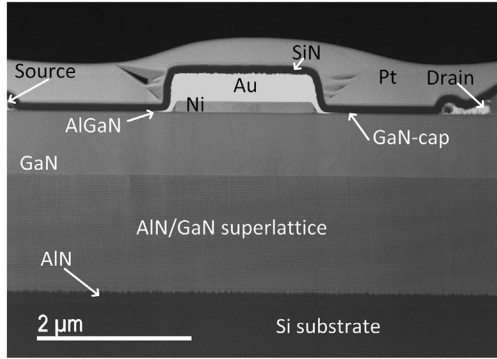

Fig. 1. High angle annular dark field (HAADF) image of an AlGaN/GaN-on-Si high electron mobility transistor.

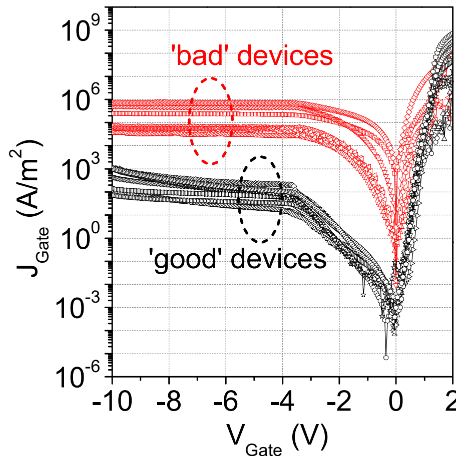

Fig. 2. J_{Gate}-V_{Gate} curves (direct current, static) of bad devices (red) and good devices (black), measured at $V_{Drain} = 0\,V$ at room temperature. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

fabricated, since their leakage current is very high, and therefore the failure time can be considered as $t_F = 0$. For good devices, we have carried out high temperature reverse bias tests and reported the results in [6]. In this test, the good devices do not experience any increase of the leakage current for > 500 h. Instead, devices fail due to a decrease of the maximum drain current, which can be explained by pit formation at the gate-edge. A similar failure mechanism was also observed for good devices stressed in the on-state, as we have also reported previously [7].

We employed various characterization techniques to understand the origin of high leakage currents in bad devices. Apparent zero-bias Schottky barrier heights (ϕ_{B0}) were extracted from J_{Gate}-V_{Gate} curves, photon emission microscopy was used to locate defects, transmission electron microscopy (TEM) was used to characterize the structure of defects, and electron energy loss spectroscopy (EELS) was used to characterize the chemical composition of the defects.

3. Results and discussion

We calculated the apparent zero-bias Schottky barrier height, ϕ_{B0}, using Eq. (1) [14],

$$\phi_{B0} = \frac{kT}{q}\ln\left(\frac{A^{**}T^2}{J_0}\right), \tag{1}$$

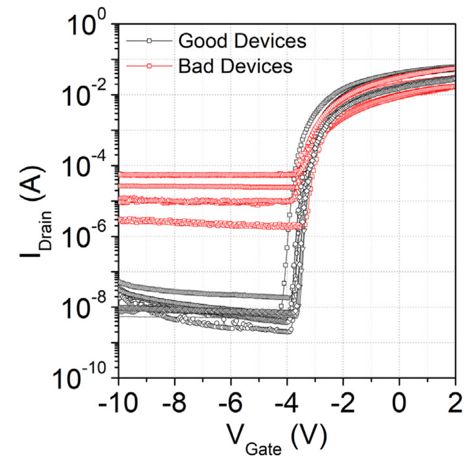

Fig. 3. I_{Drain}-V_{Gate} curves (direct current, static) of bad devices (red) and good devices (black), measured at $V_{Drain} = 10\,V$, at room temperature. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

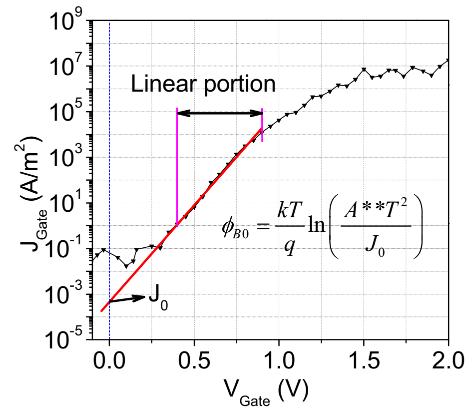

Fig. 4. Method for determination of the apparent zero-bias Schottky barrier height (ϕ_{B0}) and ideality factor (n) from a J_{Gate}-V_{Gate} curve ($V_{Gate} > 0$ V).

where q is the electron charge, k is the Boltzmann constant, T is temperature and A^{**} is the effective Richardson constant. J_0 is the reverse saturation gate leakage current density, which is obtained from a linear extrapolation of $\ln(J_{Gate})$ vs. V_{Gate} as illustrated in Fig. 4.

We also calculated the ideality factor of these devices, n, using Eq. (2),

$$n = \frac{q}{kT}\frac{\delta V_{Gate}}{\delta \ln(J_{Gate})}, \tag{2}$$

where $\delta V_{Gate}/\delta\ln(J_{Gate})$ is obtained from the inverse slope of the linear portion of $\ln(J_{Gate})$ vs V_{Gate} curve as shown in Fig. 4.

Table 1 summarizes the calculated parameters of good and bad devices. Good devices are seen to have apparent zero-bias barrier heights of $\phi_{B0} = 0.79 \pm 0.03$ eV. This is reasonably close to the value reported in the literature [15–17]. On the other hand, bad devices have substantially lower apparent zero-bias barrier heights, $0.4 < \phi_{B0} < 0.62$ eV. The ideality factor of all devices (bad and good) is $n \gg 1$. This value is commonly reported in the literature for AlGaN/GaN [17, 18]. It indicates that the forward current mechanism is not only thermal emission. Other possible transport mechanisms are direct tunnelling and trap assisted tunnelling [17]. While this suggests that the true barrier height values may not be the same with apparent barrier

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