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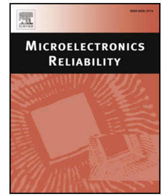

Bias voltage criteria of gate shielding effect for protecting IGBTs from shoot-through phenomena

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ABSTRACT

In this paper, we propose the criteria of bias voltage from parasitic capacitance and demonstrate the criteria in an experiment with the present IGBT. The bias voltage criteria are theoretically predicted for the new generation IGBT based on the scaling principle. For safe switching, the required gate voltage bias is predicted to be −1.2 V or less for the present IGBTs and − 6 V or less is required to completely cancel the gate noise voltage. From the IGBT design, the bias voltage of scaling IGBT requires −2 V to completely cancel the gate noise voltage.

1. New generation IGBT based on scaling principle

IGBTs are widely applied in various power electronics systems, such as electric vehicles, railways and for high-voltage direct current (HVDC) transition, and the market is rapidly expanding.

Since 2011, a new generation IGBT based on a scaling principle has been proposed and fabricated experimentally [1–4]. The IGBT features a low collector-emitter saturation voltage (V_{CE}(sat)) and low gate voltage driving. The on-state characteristics of the IGBT have been confirmed by a one-cell device experimentally [4]. The static and dynamic characteristics of larger IGBT chips have not been confirmed yet. From the viewpoint of gate structure, accurate control for the diffusion thickness of the p base layer and flouting p layer is required to lower the electric field stress of gate oxide for high reliability.

The low V_{CE}(sat) is realized by enhanced carrier accumulation because narrow mesa disturbs hole extraction. Several types of new generation IGBTs have the same feature of low V_{CE}(sat) [5, 6].

The low gate voltage driving for example 5 V instead of 15 V is realized by increased capacitance per unit area between the gate and emitter (C_{GE}) by forming of a thin gate oxide film. Only an IGBT based on a scaling principle can be driven by a low gate voltage, which saves power for gate driving in proportion to the square of the voltage swing. This means that low voltage gate driving can use the driver IC instead of the driver board. And the low voltage of the digital signal level and the driver size has the advantage of integration and/or intelligent driving [7].

However, low gate voltage driving with a low threshold voltage (V_{th}) has the disadvantage of false driving by gate noise. From this concern, the IGBT is not yet in the market. For example, the threshold voltage of the present IGBTs (scaling factor = 1) and the new generation IGBT (scaling factor = 3) is 6 V and 2 V, respectively. The V_{GE} margin from 0 V is decreased to one-third corresponding to the scaling factor. In this case, bias voltage (V_{bias}) is generally used to prevent false driving. Although V_{bias} is known by suppressing V_{GE} noise, the voltage enlarges the gate driver size because the voltage swing increases the power for gate driving and the negative voltage complicates circuit configuration. This means that the V_{bias} may lose one of the advantages of scaling IGBT.

In this paper, we propose the criteria of minimum required bias voltage from parasitic capacitance [8] and demonstrate the criteria in an experiment with the present IGBT. After that, we verify the bias voltage theoretically regarding application for the new generation IGBT based on the scaling principle.

2. Criteria of the minimum bias voltage required for the gate shielding effect

The capacitance between the gate and collector (C_{GC}) and C_{GE} is determined by the following equations:

$$C_{GC}(V_{GC}) = \frac{dQ}{dV_{GC}} \tag{1}$$

$$C_{GE}(V_{GE}) = \frac{dQ}{dV_{GE}} \tag{2}$$

The C_{GC} and C_{GE} are changed by V_{CE} and V_{GE}, respectively (see Fig. 1). V_{GC}, V_{GE} and V_{CE} are related as follows:

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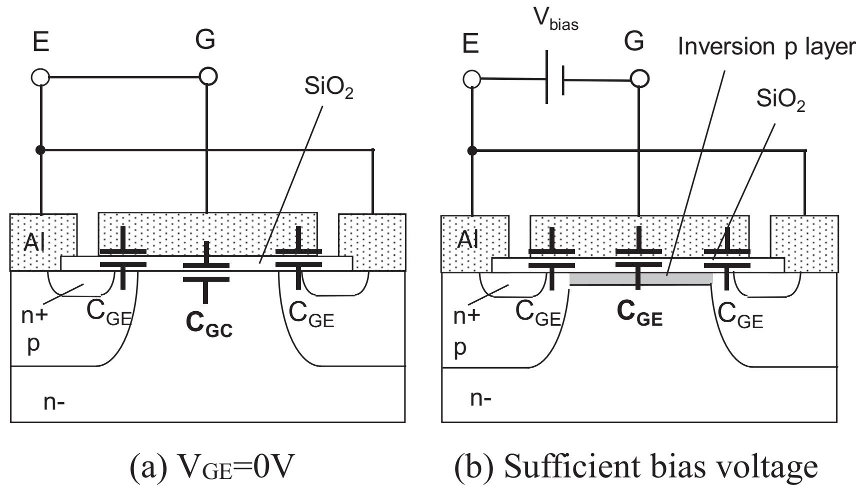

Fig. 1. Schematic view of parasitic capacitance in the emitter side of IGBT. When the bias voltage is sufficient to form a p inversion layer, C_{GC} is decreased and C_{GE} is increased.

$$V_{GC} + V_{GE} = V_{CE} \quad (3)$$

From these equations, V_{GE} under an open gate circuit is eventually expressed by the following analytical equation model as far as the C_{GC} change with the V_{CE}:

$$V_{GE}(R_G = \infty) = \frac{q\varepsilon N_B A_{GC}^2\left(\sqrt{1 + \frac{2C_{GE}^2 V_{CE}}{q\varepsilon N_B A_{GC}^2}} - 1\right)}{C_{GE}^2} \quad (4)$$

where, q, ε, NB and AGC are electron charge, dielectric constant, concentration of the n base layer and area of CGE, respectively. It is predicted from Eq. (4) that when Vbias is 0V, VGE is roughly increased in proportion to the route of VCE.

Next, we predict the V_{bias} effect from C_{GC} and C_{GE} in the experiment because the capacitance has complex V_{CE} dependence. When the bias voltage is 0 V, C_{GC} is decreased corresponding to the V_{CE} increase because the depression layer expands in the n- base region (see Fig. 2). When a sufficient bias voltage is applied for a gate shielding effect, C_{GC} is dramatically decreased because the inversion p layer covers the gate oxide film and connects the p bases. When the bias voltage is 0 V, C_{GE} is constant at a lower value because the initial diffusion layer only contributes to C_{GE} (see Fig. 3). When a sufficient bias voltage is applied, C_{GE} is constant at a higher value because the initial diffusion layer and inversion p layer contribute to C_{GE}.

The predicted V_{GE} under V_{bias} is calculated by a parasitic capacitance. These results are categorized as follows (see Fig. 4):

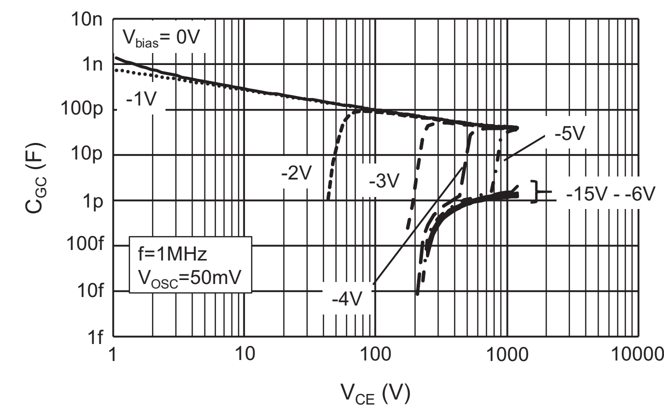

Fig. 2. Capacitance between gate and collector (C_{GC}) in our experiment. C_{GC} is decreased dramatically by the bias voltage and converged to a constant value under −6 V.

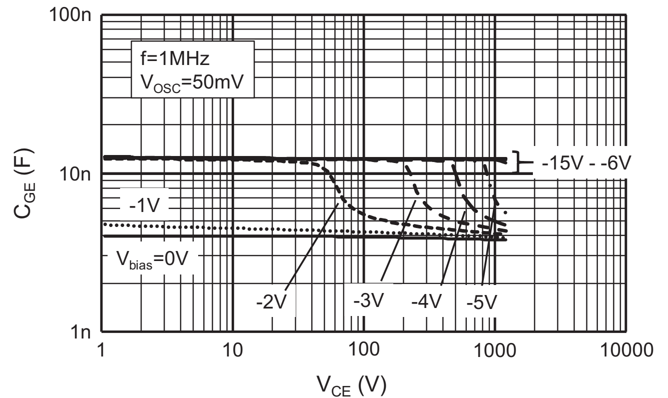

Fig. 3. Capacitance between gate and emitter (C_{GE}) in our experiment. C_{GE} is increased by the bias voltage and converged to a constant value under −6 V.

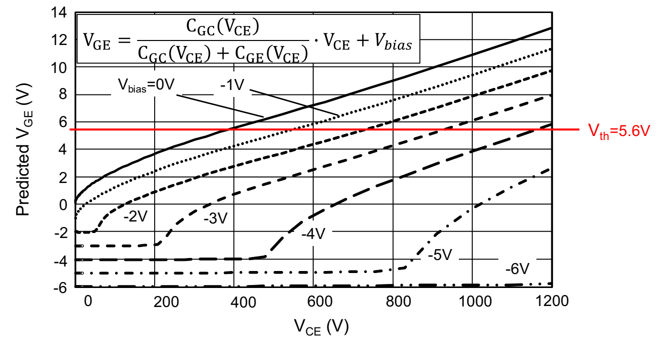

Fig. 4. Predicted V_{GE} calculated from C_{GC} and C_{GE}. The bias voltage effect is decreased by the increase of V_{CE}.

(a) $V_{bias} \geq -1$ V: V_{GE} is affected without V_{CE}
(b) -2 V $\geq V_{bias} \geq -5$ V: V_{GE} is affected depending on V_{CE}
(c) $V_{bias} \leq -6$ V: V_{GE} is not affected by V_{CE}

Increase of collector current (I_C) by false driving occurs when the V_{GE} exceeds the threshold voltage. Therefore, the criteria of the bias voltage are calculated by V_{GE} with the threshold voltage. As a result, the required bias voltage is predicted to be −1.2 V or less even if V_{CE} is assumed to be up to a DC voltage (V_{DC}) of 600 V (see Fig. 5). This time, we use planar gate IGBT in the experiment. However, the mechanism

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