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A fully digital feedback control of gate driver for current balancing of parallel connected power devices

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ABSTRACT

Parallel connected power devices such as Insulated Gate Bipolar Transistors (IGBTs) can be used to realize a system with higher current and higher power rating. However, the operation of parallel connected IGBTs is prone to unbalancing due to variation in parameters of the semiconductor devices and asymmetric parallel system. In this paper, feedback control is proposed for peak overshoot minimization as well as current balancing of parallel connected IGBTs. A fully digital feedback control (DFC) is implemented using the universal clock for balanced operation of the two parallel connected IGBTs.

1. Introduction

High power conversion and control requiring power devices with high enough voltage-current rating for power electronic converters. In order to achieve high power converter rating, devices can be connected in parallel-series to attain high voltage-current ratings. Current higher than a few kA is required for a given application with a specified voltage rating of the system. State-of-the-art devices cannot meet such requirement and a single IGBT module can supply a maximum current of few kA. Parallel connection of IGBTs is a way to match the desired current as well as the power rating. The system reliability and cost-per-ampere ratio also improved through parallelism of IGBTs [1].

Nevertheless, the operation of parallel connected IGBTs leads to unbalancing: uneven switching and uneven steady state characteristics (unbalanced dynamic and static current sharing) of devices [2]. In turn results in diminished and de-rated performance. The unbalanced behavior may cause the device operation out of the safe operating area (SOA) and subsequently, it may lead to the issue of device reliability as well as system reliability. Minimization of the IGBT current peak and current balancing through gate driver control is a possible way to avoid such problems up to an extent.

Previous works have focused on gate driver control for optimizing the switching characteristics of a single IGBT [3,4,5,6]. However, it does not automatically guarantee the balanced operation for parallel connected devices due to asymmetrical system and variation in a parameter of devices [1,7].

The active gate control strategies [7–8] are proposed for IGBTs connected in parallel based on the rising and falling edges of current. The analog signal processing circuitry is used in [7–8] to detect the current edges for the control action and achieve the balanced current sharing. In [7], the communication among the control units is essential for decentralized control action. Moreover, the delays are adjusted considering a defined set of four delay values for the case of four IGBTs. The IGBTs are subtle to change in the parameter, therefore, the gradual adjustment in delays should have to be preferred concerning system stability. Also, the unavoidable delay caused by asynchronous FPGAs clocks of the decentralized control is also a concern.

In [8], DSP-FPGA board used for the control action: FPGA board computes the rise and fall time and the active gate control action is implemented in DSP board. The active gate control comprises of rise and fall time control and peak current control. The gate signals switching times are controlled using rising and falling edges of currents, and termed as rise and fall time control. And, the monitoring of current balancing using peak amplitude of the currents is termed as peak current control.

In general, most of the active gate control strategies for parallel connected devices are extensively focused on the current imbalance from the uneven current sharing point of view. The uneven current sharing lead to the thermal de-rating of the devices [9]. Although, the currents may become almost evenly shared, that eventually cannot ensure the peak overshoot minimization of current for individual IGBTs. The overshoot in device current during switching is also a point of concern of imbalance and can lead to the SOA de-rating [9].

The peak overshoot minimization of the individual devices as well

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as even current sharing is required to improve the SOA de-rating as well as the thermal de-rating respectively. The improvement in SOA de-rating and thermal de-rating consequently approach towards the better device as well as system reliability.

The peak overshoot minimization and current balancing are the problems that need to be addressed simultaneously to enhance overall system performance. In this paper, a general concept of feedback control based on peak detection and minimization, for current balancing of parallel connected IGBTs, is presented. A fully digital feedback control of gate driver (DFC-GD) for two parallel connected IGBTs is implemented to demonstrate the current balancing. The unit step of 10 ns is used for delay adjustment. The DFC is modeled in realistic digital design simulator and implemented using Field Programmable Gate Array (FPGA) providing a universal clock for controlled operation of parallel connected IGBT.

The organization of the paper is as follows: Section 2 digital feedback control, general operating principle and implementation for two parallel connected IGBT. Section 3 the description of signal processing through ADC to feed the signal to FPGA, implementation of a noise filter and peak detection of the signal inside FPGA. Section 4 Experimental system implementation and results are explained and the conclusion is presented in Section 5.

2. Digital feedback control

2.1. General operating principle

The feedback control algorithm (see in Figs. 1 and 2) is represented for n parallel connected IGBTs. The general operating principle for the development of the DFC (see in Fig. 3) is based on the peak detection during turn-on and turn-off. Sampled digital data of IGBTs current are acquired corresponding to each pulse width modulated (PWM) signal sequence and used for the peak detection. The IGBT having maximum peak current during on-off switching is selected for control of turn-on and turn-off time.

At next step, a delay decision is executed corresponding to balancing factor criteria. According to the delay decision, the delay is adjusted to control the turn on and turn off time of gate signal to achieve peak overshoot minimization and even sharing of current. This feedback control can is defined as overshoot and balancing control (OBC).

2.2. DFC for two parallel connected IGBTs

The DFC system (see in Fig. 4) is considered to implement for two parallel connected IGBTs and drive IGBT through digital controlled GD board (see in Fig. 5) having two gate driving units. The DFC implemented in FPGA is represented through block diagram (see in Fig. 6). The measured currents are fed to FPGA through ADC. The digital signal fed to FPGA is passed through the median filter and further peak tracking logic is applied to detect the peak corresponding to each IGBT current. The amplitude of the peak value is stored in RAM.

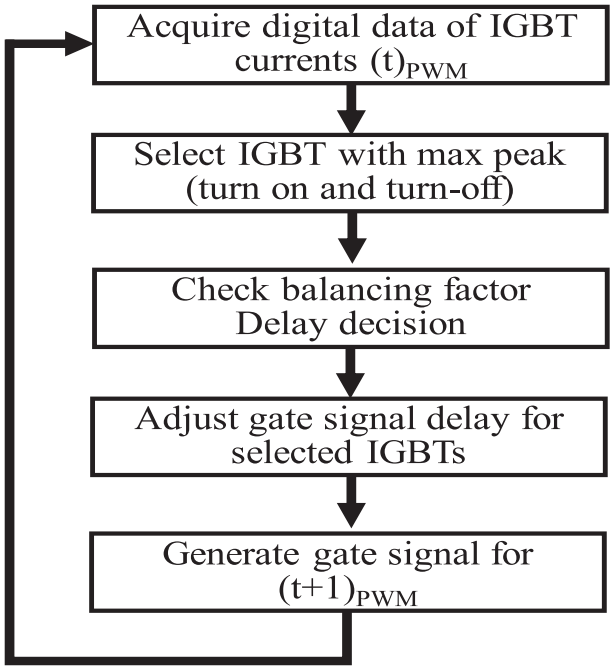

Fig. 2. Flow-chart of proposed feedback control.

The peak current is used to control the turn-on and turn-off time individually for each gate drivers. The devices with maximum and minimum peak current are selected among all the devices. And, IGBT with maximum peak current monitored by the balancing factor introduced in this paper. The balancing factor for the parallel connected IGBTs is defined as:

$$Balancing\ factor = I_{max}(t) - I_{max}(t-1) \quad (1)$$

The balancing factor and max-min selection criterion will generate a trigger signal to the counter. The counter increases the count by one unit and this is applied to the select line of the multiplexer. The desired delays are selected and incorporated into the gate signal for the next PWM switching sequence. Tolerance band can be added to balancing factor to avoid undesired delay activation in gate signal pattern.

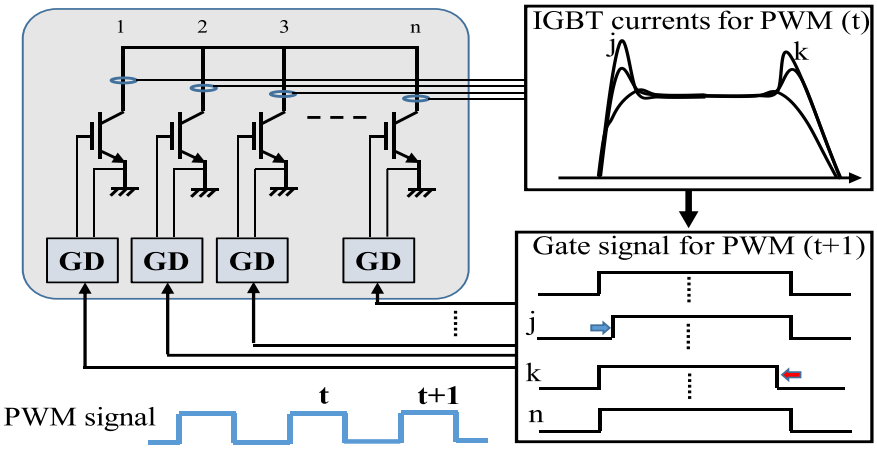

Fig. 1. Feedback control for peak overshoot and current balancing of parallel connected power devices.