Microelectronics Reliability 88–90 (2018) 519–523

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

A multi-port thermal coupling model for multi-chip power modules suitable for circuit simulators

Z.X. Wang*, H. Wang, Y. Zhang, F. Blaabjerg

Department of Energy Technology, Aalborg University, Aalborg, Denmark

ARTICLE INFO

Keywords:
Thermal model
Multi-chip power module

ABSTRACT

This paper investigates two compact thermal model representations for multi-chip power modules, namely the thermal impedance matrix model and the thermal admittance matrix model. The latter can shape a multi-port thermal network without controlled temperature sources, and can be readily implemented in circuit simulators. The mutual transformation between the two models and their relationship to parameters in the multi-port network are revealed. In addition, practical tips for thermal model parameter extractions based on temperature measurements and curve-fitting are discussed. The multi-port thermal model is verified by simulations and experimental results. It confirms that more accurate temperature estimation can be achieved compared with the thermal model without the thermal coupling effect.

1. Introduction

In order to overcome the size constraint and to increase the power density, power electronics is moving towards a more compact multi-chip package [1], which introduces thermal and reliability concerns [2]. Thus, thermal behavior has to be modeled. The thermal modeling of discrete devices has been extensively studied [3]. However, for power modules with multi-chips, the thermal coupling effect has to be taken into account [4, 5]. This issue can be addressed by a compact thermal model (CTM) [6], which can be represented by two means. One is the thermal admittance matrix [7] as a form of star-shaped model, and its fully mathematical criteria is reported in [8]. Another one is the thermal impedance matrix [9]. As shown in Fig. 1, thermal admittance matrix based thermal model is a multi-port network with different sources of the power losses. As shown in Fig. 2, thermal impedance matrix based thermal model includes power loss controlled temperature sources. Therefore, the model presented by the thermal admittance matrix is easier to be implemented in circuit simulators. On the other hand, the thermal model defined by the thermal impedance matrix is more suitable for large-scale analytical calculation, such as the temperature estimation for long-term mission profile. Nevertheless, it is lack of study on how to convert the parameters between these two kinds of models.

In addition, as mentioned in [10], the thermal impedance matrix can be defined by a $N \times N$ matrix while the dimension is $N + 1$ for the thermal admittance matrix with N being the number of temperature nodes. This additional dimension is mainly caused by the ambient temperature. As a matter of fact, if a linear thermal system dominated.

by thermal conduction is assumed, the ambient temperature is a potential reference, and has no impact on the thermal description of the thermal system. In this case, the thermal model can be represented by an N^{th} order impedance or admittance matrix through the temperature rise from ambient instead of the actual temperature. This paper focuses on the thermal transformation between these two thermal networks.

2. Two thermal model representations

Taking a thermal system with 4 nodes for example, all nodes can be fully coupled and be characterized through a 4×4 thermal impedance matrix expressed as $\Delta T = \Psi P$ in Eq. (1). The impedance matrix shapes a multi-port thermal network as shown in Fig. 2. It can be seen that each temperature node has its own thermal model with the coupling point of the ambient. Moreover, controlled temperature sources are needed in this model.

$$\begin{bmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{bmatrix} = \begin{bmatrix} \psi_{11} & \psi_{12} & \psi_{13} & \psi_{14} \\ \psi_{21} & \psi_{22} & \psi_{23} & \psi_{24} \\ \psi_{31} & \psi_{32} & \psi_{33} & \psi_{34} \\ \psi_{41} & \psi_{42} & \psi_{43} & \psi_{44} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{bmatrix} \quad (1)$$

where ψ_{ii} is the thermal impedance between node i and the ambient T_a; P_i is the power loss at node i; ψ_{ij} is the thermal impedance between node i and node j representing the thermal coupling effect between them; ΔT_i is the temperature difference between node i and the ambient.

* Corresponding author.
E-mail address: zho@et.aau.dk (Z.X. Wang).

https://doi.org/10.1016/j.microrel.2018.06.031
Received 31 May 2018; Accepted 25 June 2018

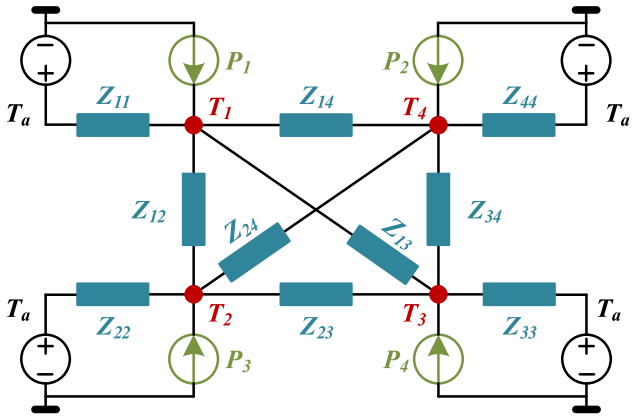

Fig. 1. Multi-port thermal coupling network derived from the thermal admittance matrix with 4 driving nodes.

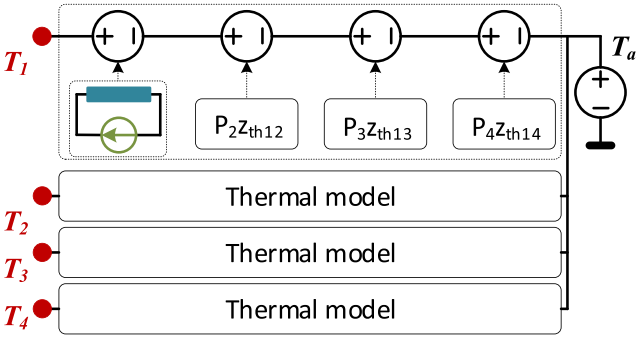

Fig. 2. Multi-port thermal coupling network derived from thermal impedance matrix with 4 driving nodes.

It should also be noted that the thermal impedances ψ_{ij} do not correspond to the parameters Z_{ij} in the multi-port thermal network defined by the thermal admittance matrix. Specifically, the power dissipation P_1 totally goes through ψ_{11} to generate the temperature rise of node T_1 in the thermal impedance matrix based model. However, in the multi-port thermal network shown in Fig. 1, the power is transferred through all available paths. Thus, the parameter ψ_{ij} is a combined effect of all elements in the multi-port thermal network. To explore the relationship between the two matrixes, matrix transformation has to be conducted. For simplification, thermal conductance Y_{ij} is used instead of the thermal impedance Z_{ij}, which is the reciprocal of Y_{ij}.

Taking node T_1 in Fig. 1 for example, the heat flow balance equation is

$$\begin{pmatrix}(T_1 - T_2)Y_{12} + (T_1 - T_3)Y_{13} \\ + (T_1 - T_4)Y_{14} + (T_1 - T_a)Y_{11}\end{pmatrix} = P_1 \tag{2}$$

where Y_{ij} is the thermal conductance between node i and j, and $Y_{ij} = Y_{ji}$. Rearrange Eq. (2) to make sure that all temperatures are referred to the same reference T_a,

$$\begin{pmatrix}(Y_{11} + Y_{12} + Y_{13} + Y_{14})\Delta T_1 \\ - Y_{12}\Delta T_2 - Y_{13}\Delta T_3 - Y_{14}\Delta T_4\end{pmatrix} = P_1 \tag{3}$$

Taking heat balance equations of all 4 nodes into account,

$$\begin{bmatrix}P_1 \\ P_2 \\ P_3 \\ P_4\end{bmatrix} = \begin{bmatrix}K_{11} & K_{12} & K_{13} & K_{14} \\ K_{21} & K_{22} & K_{23} & K_{24} \\ K_{31} & K_{32} & K_{33} & K_{34} \\ K_{41} & K_{42} & K_{43} & K_{44}\end{bmatrix}\begin{bmatrix}\Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4\end{bmatrix} \tag{4}$$

where $K_{ii} = \sum_{j=1}^{4} Y_{ij}$, $K_{ij} = -Y_{ij} (i \neq j)$. The matrix equation can be further simplified as $P = K\Delta T$, in which K is the thermal admittance matrix, and the relationship $\Psi = K^{-1}$ can be derived. It can be extended to thermal systems with N nodes by only changing the range of subscripts i and j to N.

Based on the above analysis, the relationship between the parameters Ψ and Z of the two multi-port thermal networks is,

$$\begin{cases} K = \Psi^{-1} \\ Y_{ii} = \sum_{j=1}^{j=N} K_{ij},\ Y_{ij} = -K_{ij} (i \neq j) \\ Z_{ij} = \frac{1}{Y_{ij}} \end{cases} \tag{5}$$

Note that none of the parameters ψ_{ij}, K_{ij}, and Z_{ij} has physical meaning. All of them are a general thermal description between nodes. In addition, thermal parameters Z_{ij} may contain negative values if Foster RC model is used to fit the thermal transient, which could lead to convergence issues [11].

Moreover, to distinguish the two multi-port thermal coupling networks and their potential applications, their features are summarized as below:

1) The multi-port thermal network defined by thermal admittance matrix can be easily implemented without a controlled temperature source.
2) The multi-port thermal network derived from the thermal impedance matrix can shape independent thermal model for each temperature node, and no coupling exists among nodes. Thus, it is suitable for fast temperature estimation with large-scale data processing, such as the junction temperature estimation for long-term mission profile.

3. Thermal impedance matrix extraction

The thermal impedance matrix is usually obtained from either simulation or experiment. The approach is to apply a step power on each chip of interest until the thermal steady-state is achieved. The on-state voltage drop and the current going through the device under test (DUT) are tested for power loss calculation before switching off the power supply. Then the temperature cooling curves of all chips are recorded simultaneously. In this paper, a four-chip half-bridge IGBT module F4 50R12KS4 from Infineon is used as the DUT. Note.

that to facilitate the temperature measurement by thermal camera as shown in Fig. 3, the IGBT has to be black painted. Based on the tested power loss and temperature responses, the self and mutual thermal impedances can be calculated by the temperature rise over the constant power dissipation. They can be further fitted into a series of Foster RC network and finally get the thermal impedance matrix Ψ. Based on Ψ and the thermal model transformation method in Section 2, the thermal admittance matrix K can be obtained. Figs. 4 and 5 show part of the thermal parameters of ψ_{ij} and Z_{ij}. As can be seen, different from the thermal impedance matrix with all values of its Foster model being positive, certain negative values can be expected for the Foster model of the thermal admittance matrix parameters. In addition, the thermal impedance matrix ($t = 1000$ s) is illustrated in Eq. (6), in which the symmetrical characteristics ($\psi_{ij} = \psi_{ji}$) can be observed with a negligible difference caused by the measurement and the nonlinearity in the system.

$$\Psi_{t=1000s} = \begin{bmatrix}0.5880 & 0.2244 & 0.3058 & 0.2961 \\ 0.2228 & 0.5353 & 0.2466 & 0.2452 \\ 0.2974 & 0.2512 & 0.6172 & 0.2933 \\ 0.2954 & 0.2466 & 0.3092 & 0.5995\end{bmatrix} \tag{6}$$

Moreover, several practical tips are listed for the parameter extraction through experiments:

1) Cooling curve is preferred since a constant power dissipation is