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Automated pre-placement phase as a part of robust analog-mixed signal physical design flow

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ABSTRACT

A new pre-placement phase of integrated circuits (IC) analog-mixed-signal (AMS) physical design flow, introduced in this paper, automatically sorts electrical devices used in planar IC technologies according to their topological, structural and electrical properties. The presented design phase replaces human labour and allows to save design time and prevent human mistakes. Software implementation of the proposed method works with virtual objects of layout instances which are moved only once at the end of the script when creating the final pre-placement matrix. Algorithm complexity is decreased by a new way of virtual objects matrix indexing. The automatic pre-placement phase has been used during design of AMS circuits in 160 nm BCD8sP and SOIBCD8S technologies from STMicroelectronics and has been faster in the range of 3164 to 20099 times compared to manual sorting. The estimation of ratio between manual sorting time and automatic pre-placement time shows a growing time saving with increasing circuit complexity compared to standard layout flow. The introduced enhanced layout flow is able to prevent a creation of hardly detectable errors occurring at the beginning of AMS physical design, especially the wrong bulk connection errors of semiconductor devices. The automatic pre-placement phase saves hours of reworks and speeds up the entire design process.

1. Introduction

The design of semiconductor analog or analog-mixed signal (AMS) integrated circuits (IC) can be divided into several subsequent and mutually dependent steps. A very important one, out of those is the physical implementation of designed circuit topologies, in other words, integrated circuit layout which is in majority of companies usually done by a person other than the one working on microelectronic circuit design and its simulations. This work-partitioning is essential to achieve desired project timing.

The designed circuit topologies are usually not mature, not enough verified when the process of layout starts and as a deadline for sending lithographic data to a plant is getting closer, arising time pressure has to be dealt with. Thus the right timing of all the layout tasks is crucial from the beginning. Implementation of procedures and methods for saving time and preventing human failure can reasonably influence final time-to-market [1].

In practice, AMS physical design of all analog blocks and the whole ICs created by the Analog-on-Top approach is still handmade. No fully automated AMS physical design flow is accepted by physical design engineers because this has not achieved the quality of manually crafted physical designs, so far [2]. However, physical design engineers like using assistant functions [3] published in Refs. [4–6] facilitating work on individual design steps. The assistant functions can save a considerable amount of valuable time, save human labour, and eliminate some types of errors such as non-compliance with the design rules, wrong metallic interconnections, or wrong current capability and too high resistance of metallic wires. The most critical place to create fundamental errors passing through the entire physical design flow is the step before the placement itself when even hundreds of individual instances are sorted manually. These errors are usually detected only during the final verification and their detection returns the physical design to the beginning. Presence of these errors leads to a wrong area estimation, and thus it can affect the surrounding blocks as well. Additionally, the finished placement must be changed in most cases as well as all follow-up phases. Works and tools published so far do not solve this problem. Therefore an algorithm automating this phase named a pre-placement phase has been proposed. Using this automated algorithm, the pre-placement phase is accelerated, the entire physical design flow is faster, and the errors caused by manual work are eliminated.

The pre-placement phase is governed by rules which are derived

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from physical structures of devices used in a semiconductor technology and from usually used building blocks in IC design. Compliance with the rules is the fundamental prerequisite for flawless placement. Outputs of the proposed algorithm are groups of instances sorted according to the rules. Then the physical design engineers do not have to work with a large number of instances but they only work with a smaller number of defined groups which improves the clarity of the whole design and thus its quality. In a case of using an automatic analog placer, the proposed algorithm works as a generator of fundamental constraints without their definition is not possible to perform correct automatic placement [2].

The paper is organized as follows. Section 1 follows with description of the state of the art and new contributions. The principle of the new physical design phase is introduced in Section 2. For real use in IC design, principle implementation in a well-known CAD environment is described in Section 3. Finally, the benefits of the presented method are assessed in Section 4.

1.1. State of the art

In the early years of integrated circuitry design and production a lot of time was spent on an inspection of the semiconductor structures drawn on tracing paper as all geometrical parameters were checked manually by rulers and protractors. As time passed this inefficient technique was replaced by computer aided design (CAD) applications which are beneficial for both design and inspection of the semiconductor structures. Development of CAD applications for IC physical design began in the second half of the 20th century [7,8]. Today's CAD systems [4–6] allow modifications of physical design flow and implementation of new algorithms. Unlike digital synthesis and implementation tools, AMS physical design still remains a handwork. Several automated tools for analog layout were presented [2]. Some of them are capable of good quality routing, some of them help with generation of devices, unfortunately still there is no tool widely commercially used for analog placement. There are two main reasons for this situation. At first, placement of AMS circuits requires much more constraints compared to digital ones. As described in Ref. [3], these constraints can be implicit or explicit, and in AMS physical design flow it is very difficult to express all of them explicitly to be then accessible for algorithmic processing.

The second obstacle in AMS physical design flow, well stated in Ref. [9], is somehow a reluctance of analog designers to use a complete automated analog flow. They are missing some kind of “aesthetics” in an automatically proceeded layout. Aesthetics which enables human beings to verify with a naked eye if electrical and matching requirements are met. Instead, analog designers prefer small automated steps, using so-called in-design assistants that design environments from different vendors are full of. Designers can use them for time consuming tasks but keep the control of the whole layout. Proposed flow directly formulates the very essential constraints for placement right in the explicit way while working as an in-design assistant at the same time.

In the final phase of physical design, lithographic design shapes are transformed into text or vector files and their geometrical and electrical parameters are checked by automatic algorithms [10]. The principle of these checks has remained similar up to now, of course modern and more efficient algorithms [11,12] are used in the contemporary CAD environments. Unfortunately, this saves time only during the inspection at the end of design.

However, another amount of time can be saved by anticipating human failure in early stages of layout. Again, automatic algorithms implemented in CAD environment can do a part of the job. They are able to lay out simple integrated circuits [13], typical circuit structures [14,15], basic analog building blocks [16] or to optimize floorplan using multi-objective optimization algorithm based on topological benchmark [17]. They can replace lengthy and complex manual work which humans are most likely to make a mistake in. And if they keep respecting particular stages of integrated circuitry layout, these algorithms can be appropriately combined, so results of one algorithm can be used as an input for another one. The analog layout flow is then becoming partially automated.

Numerous works describing almost fully autonomous physical design synthesis have been published. The approach [18] describes automatically generated constraints used for an automatic placer and then for an automatic router. Another automatic physical design flow [19] takes into account influence of each device reshaping and is focused to find an optimal layout by applying a non-slicing placement algorithm and numerical (SPICE) simulation to evaluate device sizing procedure and influence of layout parasitics.

Automated methods [18,19] look very promising, but there are several drawbacks which limit their usage in practice. The core of these methods is an extraction of matched structures such as current mirrors, cascaded current mirrors, and differential pairs. High precise designs use trimmed structures which contain a number of pass-gates and switches to be able to configure required circuit parameters. Also in low power designs used in mobile applications and in the Internet of Things (IoT), the power consumption is very optimized. Due to this need, AMS circuits contain switches disconnecting dedicated parts. In high reliable design, the negative bias temperature instability (NBTI) [20] and the positive bias temperature instability (PBTI) [21] phenomena are taken into account. Therefore inputs of differential amplifiers are usually reconfigurable. The additional switches do not allow simple detection of basic analog structures. This is another reason why until today there is no universal tool for automated AMS physical design synthesis and AMS physical designs are still made manually.

1.2. New contributions

This paper describes an automatic algorithm applicable for sorting electrical devices with respect to their electrical parameters. The algorithm here presented introduces an automated design phase of the analog IC physical design, as it forms groups of topologically, structurally and electrically corresponding devices after these had been generated coming from the electrical scheme. The developed algorithm directly replaces slow manual work inevitable at the beginning of physical design, the sorting of devices into described groups and facilitating the analysis of circuit structures for physical designers. When keeping precise circuit parameters is becoming crucial, this phase of high quality AMS layout cannot be left out. In robust designs, results of the proposed algorithm can be used for very fast and precise area estimation, manual placement as well as basic constraints for automatic placers.

There are several reasons to use this automatic algorithm. The first one is a prevention of human failure. In standard flow, numerous types of mistakes, even those made in the very beginning of layout, can only be detected at the end of layout when the whole circuit is being checked. Reasonable time is then usually required to fix an issue. The implementation of the presented algorithm can not only save this repair time but also considerable time necessary for the initial manual sorting of electrical devices. This algorithm helps reducing total time necessary for layout completion which also means that the cost of development can be lowered. That is the most important advantage.

The proposed method allows the creation of robust ICs which are used in automotive, plane or space applications. In these designs, parasitic thyristor structures have to be eliminated. Latch-up of these structures inside ICs causes their wrong behaviour or total damage unacceptable in above-mentioned applications. Space applications and applications operating in a harsh environment have to be resistant to ionizing radiation which may cause system malfunctions or damage by single-event effects [22]. The presented algorithm allows to use physical radiation-hardening technique for ICs manufactured on both substrate types, on the silicon on insulator (SOI) substrates or on the usual bulk semiconductor silicon wafers.