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A loadless 6T SRAM cell for sub- & near- threshold operation implemented in 28 nm FD-SOI CMOS technology

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ABSTRACT

Most ultra low power SRAM cells operating in the sub and near threshold region deploy 8 or more transistors per storage cell to ensure stability. In this paper we propose and design a low voltage, differential write, single ended read memory cell that consists of a total of 6 transistors. The innovative idea is to bring the loadless 4-transistor latch into the realm of low voltage memory cells by exploiting features of the 28 nm FDSOI Process and by adding a 2-transistor readbuffer with a footer line. Stand-alone and on a system level, the cell is stable during read, write and hold operations and it has great write-ability due to its differential write and loadless nature. The single NWELL option in 28 nm FD-SOI allows the loadless core to have minimal device widths while greatly improving the time it takes to evaluate the read bit-line. The cell has, in this paper, been used in a 128 kb (2^{17}) SRAM in a 16 block configuration exploring 3 different types of logic libraries for the peripheral logic of the system. Depending on the application, the IO-peripheral logic may be implemented using either high threshold voltage transistors or low threshold voltage transistors in where the power consumption of the 128 kb system was found to range from 1.31 μW to 71.09 μW, the maximum operational frequency lies within 1.87 MHz and 14.97 MHz while the read energy varies from 13.08 to 75.21 fJ/operation/bit for a supply voltage of 350 mV. The minimum retention voltage of the loadless SRAM cell is found to be 230 mV covering 5σ of variation with Monte Carlo simulations.

1. Introduction

The number of devices connected to the Internet is predicted to increase from 12.5 billion in year 2010 to 50 billion within year 2020 by Cisco [1]. The explosive growth of on-line devices motivate advances in sensor node design as well as in data center efficiency. To enable this growth, an important area of research is energy efficiency for battery driven devices [2] and power efficiency in data center solutions to mitigate the dark silicon effect [3].

Static Random Access Memories (SRAMs) are heavily utilized in microprocessors as register files, instruction memories and data memories. Thus, SRAMs account for significant fractions of on-chip area and power & energy -consumption in microprocessors and therefore also in data centers and in sensor networks. To improve the energy & power efficiency in sensor networks and in data centers, innovations are needed within the field of SRAM design.

By designing digital circuits to operate in the sub- and near-threshold region one may trade operational speed for power consumption. Typically there is a sweet-spot for the supply voltage in terms of energy per operation that is normally located around the threshold voltage of the transistor, it is called the minimum energy point (MEP) [4]. For SRAM memories, the voltage where the MEP is located is typically higher than that of static CMOS logic [5], yet it is so low that operation on the MEP raises quite a few challenges where ensuring stability of all bit-cells in the memory arrays during hold, read and write operations are among the main concerns.

To lower the minimum operating voltage (V_{min}) of SRAM cells, architectural innovations are needed. Today most SRAM cells that are made for low supply voltages are made stable by adding read and write assists to the conventional 6T SRAM cells thereby increasing the number of transistors per cell to 8T [6], 9T [7], 10T [8], 11T [9] 12T [10], 14T [11] and even higher numbers. In applications where large amounts of embedded memory is needed, having such large transistor count per memory cell and thus proportionally large area per memory bit leads to infeasible total area consumption. In this paper we therefore propose a 6T SRAM cell architecture that is suitable for low voltage applications. The cell has a retention voltage of 230 mV, and for a 2^{17} bit (128 kb), 16 block, SRAM configuration with I/O peripheral logic made from a custom, low leakage library, a leakage per bit of 9.99 pW and energy per bit accessed in a 64 bit word read-operation of

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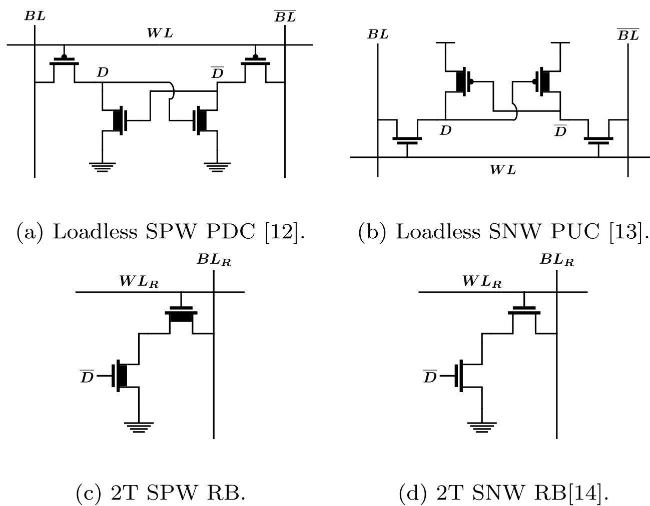

Fig. 1. a) & b): Loadless single p-well (SPW) pull down (PD) and single n-well (SNW) pull up (PU) cores that are prone to read failures at low V_{DD}. c) & d): read buffers to mitigate the problem.

13.08 fJ.

In section 2, the proposed cell architecture is explained in detail, the cell sizing is elaborated with respect to the cell's hold and read stability of the cell together with the cell's write ability. The simulation setup is also listed in the same section. Following is the results in section 3 in terms of well established figures of merit for memory systems. The results are discussed in section 4 and conclusions are drawn in the same section.

2. Methodology

2.1. Memory cell design, stability & reliability

2.1.1. Memory cell design

To achieve a low transistor count a loadless 4T cell core was created as shown in Fig. 1(a) by the Nippon Electric Company (NEC) for ultra-high density SRAM macros [12]. NEC based their work on the 4T NMOS memory cell with pull up resistors that has dominated the standalone SRAM market. By removing the resistive loads that requires a dedicated process step, NEC introduced the 4T loadless cell for embedded SRAM applications. The loadless pull down core structure in Fig. 1 (a) operates on a principle of high leakage PMOS pass-gates and low leakage cross coupled NMOS pull down transistors. Data retention is achieved by pre-charging the bitlines to VDD whenever the SRAM is idle. The high leakage PMOS pass gates then provides the cross coupled NMOS pair with supply current. Two design criteria for robust data retention in loadless pull down SRAM cells exist:

- The off current of the NMOS transistors should be significantly lower than the off current of the PMOS transistors in order to store a logic high.
- The on current for the NMOS should be significantly higher than the off current of the PMOS transistors in order to store a logic low.

Similarly for the loadless pull up core in Fig. 1 (b) [13], the bitlines are pre-charged to ground potential whenever the SRAM cell is in the hold state. To retain the stored data, the high leakage NMOS pass gates pulls sufficient supply current from the cross coupled PMOS pair. We have the following two design criteria for data retention:

- The off current of the PMOS transistors should be significantly lower than the off current of the NMOS transistors in order to store a logic high.
- The on current for the PMOS should be significantly higher than the off current of the NMOS transistors in order to store a logic low.

Both cell cores in Fig. 1 (a) and (b) were at first implemented on a schematic level. To fulfill the design criteria itemized above: Low threshold voltage PMOS devices (LVTPFETs) were used as access gates and regular threshold voltage devices (RVTNFETs) were used as pull down devices for the loadless pull-down cell. And for the pull-up cell, LVTNFETs were used as access gates and RVTPFETs were used as pull up devices. Exploiting the flip-well structure of the LVT devices in 28 nm FD-SOI allows the entire bitcell to be placed in a single P-well and a single N-well for the pull-down SRAM cell and for the pull-up cell respectively. Simulations proved that both loadless cores failed to retain their memory state during read operations for a supply voltage of 350 mV. The differential read, differential write -cores were thus made into single ended read, differential write -cores by adding the single ended read buffers in Fig. 1 (c) and (d) [14]. The transistor count is increased from 4T to 6T to completely isolate the memory cells during read operations, equating the read margin to the hold margin for both cores.

The main issue with operating the conventional read buffer architectures in the near-threshold and subthreshold -regions, is the low I_{on}/I_{off} ratios of the transistors in the read buffers. The low on-current and relatively high off-current makes it difficult to distinguish the voltage differential on the bitlines caused by the non-selected rows in the same column from the read voltage differential generated by the accessed read buffer. Fig. 2 illustrates the bitline leakage problem. The higher the bitline is, in terms of column bitcells, the more cells are not accessed but still contribute to pulling down the pre-charged capacitance which again makes it more difficult to distinguish between logic 1s and 0s for the read-out logic. Since the readout buffer is single ended and, let us say that it is connected to the $\overline{D}$ node in the loadless SRAM core, the worst case scenario occurs when the accessed cell has $D = High$ with a corresponding $\overline{D} = Low$ and if all other cells in the column have $D = Low$, $\overline{D} = High$ ie. open buffer transistors and closed access transistors. The bitline is in this case supposed to retain its value since the accessed read buffer transistor is turned off, however BL_R ends up getting discharged by the sum of leakage currents from the unaccessed cells. This is also furthermore amplified by the impact on the I_{on}/I_{off} ratios from process voltage and temperature (PVT) variations. Fig. 3(a) depicts that the I_{on}/I_{off} ratio of an LVTNFET transistor varies by several orders of magnitude over the industrial temperature range from $T = -40\,^{\circ}\mathrm{C}$ to $T = 85\,^{\circ}\mathrm{C}$ with a supply voltage variation range of ± 10%. Process and mismatch variation adds even more variation to the I_{on}/I_{off} ratio which can be seen in (b).

To be able to perform read operations in the worst case read

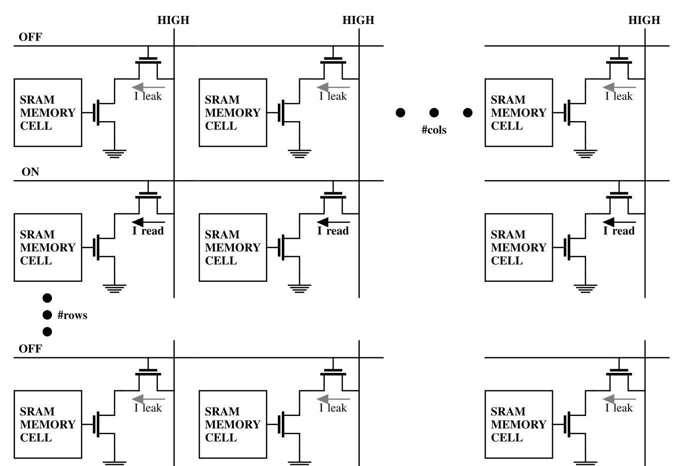

Fig. 2. Read BL problem for conventional 2T read buffers.

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