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A 2.4 mW 2.5 GHz multi-phase clock generator with duty cycle imbalance correction in 0.13 μm CMOS

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ABSTRACT

A high-speed multi-phase clock generator with duty cycle imbalance correction is proposed. Multiplexers are added between every two registers to correct the imbalance, hence to reduce the deviation of duty cycle and magnitude among multi-phase clocks while maintaining a high operating frequency and low power consumption. An eight-phase 12.5% duty cycle clock generator is designed and fabricated using a 0.13 μm RF CMOS process. It's able to generate multi-phase clocks with less than 1° duty cycle imbalance and has a measured operating frequency up to 2.5 GHz with a maximum power consumption of 2.4 mW from a 1.2 V supply while occupying a silicon area of 65 μm × 100 μm.

1. Introduction

Multi-phase clock generator at gigahertz range has been one of the key building blocks in high-speed applications such as radio-frequency integrated circuits and data converters [1–9]. In the noise cancelling receiver, e.g., where the RF signal is down-converted by the multi-phase clock signals, accurate multi-phase signals are crucial to conversion loss and noise figure [1,5,8,9]. Thus, an I/Q imbalance calibration is often utilized to overcome the image rejection issues caused by phase/gain mismatch of high-frequency clock generator. The clock generator providing non-overlapping multi-phase clock signals with low phase and duty cycle imbalance would relax the calibration requirements. A single line of delay units, used as an open-loop or injected-locked ring oscillator, has been a popular solution for its high-speed and good phase accuracy [2,3,6,7], while solving the power consumption problems in a closed-loop system simultaneously [4]. Unfortunately, undesired phase overlapping exists in two adjacent output signals of the 50% duty cycle multi-phase clock generator, making it less attractive in the applications of the noise-cancelling receiver. A popular way to create non-overlapping clock signals is making every two signals with 45° phase shift AND-ed together [8,9]. However, the eight AND-gates would occupy and consume additional silicon area and power. Thus, the shift register-based divider is designed to obtain a 12.5% duty cycle non-overlapping phase signals directly [1]. Nevertheless, different loads in the registers would cause phase and duty cycle imbalances among all the eight outputs with small overlapping in the practical implementation. When the non-ideal eight-phase pulses are employed as LO signals to drive the passive mixers, the distorted down-converted signal would seriously affect the performance of the receiver [1,8,9]. In this paper, a new multi-phase clock generator is proposed to solve this issue while maintain a high operating frequency and a low power consumption.

2. Design consideration

The design considerations of the multi-phase clock generator in a noise cancelling receiver include the operating frequency, power consumption as well as phase and duty cycle balance. As illustrated in Fig. 1, four stages of negative-feedback connected delay cells with injected signal are used to generate 50% duty cycle clocks with 45° phase-shift. To obtain non-overlapping multi-phase clocks, additional logical circuits that introduce additional power consumption and silicon area are desired [3,8,9]. A divider based on linear feedback shift register is proposed as shown in Fig. 2 [1]. In this design, the start-up register cell holds an initial logic state of HIGH, while the other signals remain logic LOW. A negative clock transition moves this logic HIGH along each register while a positive clock transition sets the output to be logic LOW. With external differential clocks at four times of the operating frequency, non-overlapping clocks with eight phases are hence generated. Therefore, the shift register-based divider maintains a good balance among non-overlapping, high speed and power consumption [1–3].

However, a start-up circuit is needed to generate the very first logic HIGH as the duration of start signal can't be longer than the external clock period. Otherwise there will be more than one logic HIGH passing

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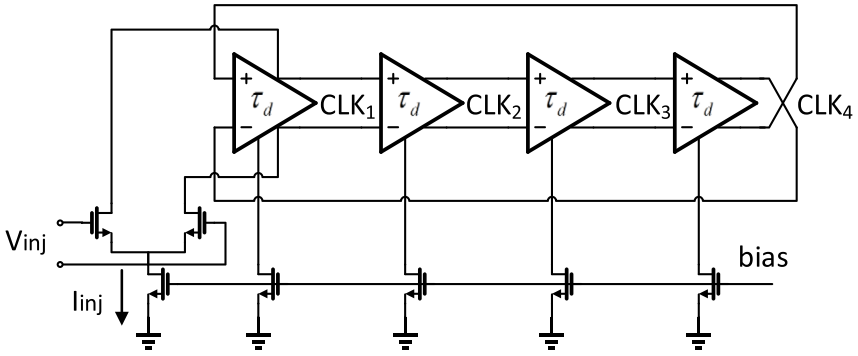

Fig. 1. The conventional 8-phase clock generator based on the injection locked ring oscillator.

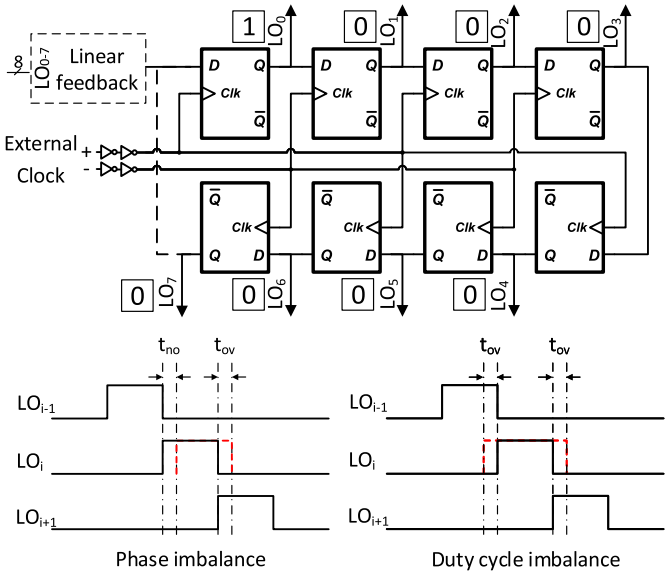

Fig. 2. The 12.5% duty cycle clock generator based on the shift-register divider in Ref. [1].

through the register loop. Consequently, the shift-register-based divider is actually a larger loop with a linear feedback circuit as a signal injection point which on the other hand breaks the load balance in the original shift register loop. Furthermore, the layout implementation of a loop architecture is of a poor symmetry due to different interconnects between every two registers. The phase and duty cycle imbalance among the outputs signals caused by the above-mentioned reasons results in undesired overlapping between adjacent phase, leading to unnecessary large magnitude and phase error of the IF signals in a RF system.

3. Proposed design

The proposed work is an improved topology from Ref. [1] with the registers designed according to its rules, as shown in Fig. 3. The input signal *D* pulls down the internal node Q_b whose previous stage is logic HIGH. Hence the internal node Q_b turns on the pMOS transistor M_{p3} to store the input signal. Then negative transition of the clock propagates the logic HIGH to the register's output *Q* and pass it along. Similarly, the positive transition of the clock pulls *Q* to logic LOW and the pre-charge signal *HF* turns Q_b HIGH before the next clock cycle. In this work, the multiplexers are inserted between every two registers as the load balance circuits forming a balanced register loop. The first multiplexer controlled by signal *SEL* offers two signals as the input of the start-up register cell. When all the register outputs are logic LOW, the linear feedback circuit generates a short duration of start-up signal and pass it to the first register. Once the logic HIGH appears in the register loop, the linear feedback circuit makes the last register's output transparent to the first register's input by controlling the signal *SEL*. Thanks to the dummy multiplexers controlled by logic LOW, all the loads and the layout interconnections of the registers are well balanced. Proper sizing of the transistors is performed at both schematic and layout levels so that the generator can work robustly over the variations of process corners, temperature, and supply voltage while a low power consumption is maintained.

The layout sketch of the proposed multi-phase clock generator is shown in Fig. 4. The linear feedback circuit is located in the center of the register loop with a multiplexer on both sides so that the difference among the registers' output line is minimized. Since the operation of the circuit is subject to the quality of the input differential clock, clock skew has a significant impact on the multi-phase clock generator. In this work, the red lines are clock signal distribution network on the high level mental layer with an equal length from clock input point to every register to maintain the highest level of symmetry.

With the circuit-level correction and the well-designed layout, an eight-phase clock generator is implemented in a 0.13 μm CMOS technology as a design example. When a multi-phase clock generator works at GHz range, the rising and falling times would not be sharp enough. In this prototype, the multi-phase clocks are generated by the logic HIGH passing along the register. Therefore, the duty cycle is defined as the following equation:

$$D = \frac{t_{on}}{T} \tag{1}$$

where *D* and *T* are respectively the duty cycle and the period of multi-phase clock and t_{on} is the time span when nMOS M_{n1} is turned on.

Since the conventional eight-phase clock generator has a start-up signal injection point, the output of this register often has inevitable duty cycle deviation from the other phases, while the duty cycle deviation is greatly suppressed in the proposed multi-phase clock generator. A Monte Carlo Simulation with 1000 runs has been carried out to evaluate the duty cycle performance of the conventional and proposed clock generator, which is shown in Fig. 5.

In order to measure the duty cycle imbalance between LO_0 and LO_7, eight output buffers are designed to drive the large capacitors brought by an oscilloscope or a spectrum analyzer as illustrated in Fig. 3. Therefore, the voltage at the load capacitor is determined by the buffer's current, load capacitance and the charging time. The output buffer consists of several stages of inverters, the charging current is weakly